ERDA/JPL 954356-76/2
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DIP COATING PROCESS

Silicon Sheet Growth Development for the
Large-Area Silicon Sheet Task of the
Low-Cost Silicon Solor Array Project

Annual Report No. 1

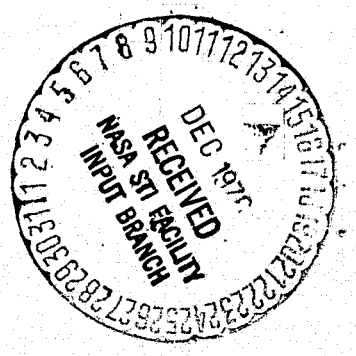
by

J. D. Heaps, R. B. Maciolek, J. D. Zook, W. B. Harrison,
M. W. Scott, G. Hendrickson, H. A. Wolner, L. D. Nelson,
T. L. Schuller and A. A. Peterson

Period Covered: 10/21/75 - 9/17/76

Published September 28, 1976

Honeywell Corporate Research Center
10701 Lyndale Ave. South
Bloomington, Minnesota 55420



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ABSTRACT

The objective of this research program is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by dip-coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon. The dip-coating methods studied were directed toward a minimum-cost process with the ultimate objective of producing solar cells with a conversion efficiency of 10% or greater.

The technique shows excellent promise for low-cost, labor-saving, scale-up potentialities and would provide an end product of sheet silicon with a rigid and strong supportive backing.

An experimental dip-coating facility was designed and constructed, and, using this facility, several substrates have been successfully dip-coated with areas as large as $25cm^2$ and thicknesses of 12μm to 250μm. There appears to be no serious limitation on the area of a substrate that could be coated.

Of the various substrate materials dip-coated this reporting period, mullite appears, at this time, to best satisfy the requirement of this research program. An inexpensive process has been developed for producing mullite in the desired geometry, thus satisfying the cost objectives of the program.

Crystallization of the coatings occurs in a manner that ensures continued nucleation from previously grown silicon, thereby producing layers with silicon grains that are many times larger than the thickness of the layer. Typical layers of 50μm thickness have single dendritic grains as large as 1mm wide tending to extend over the length of the substrate with the long dimension of the dendrite along the pulling direction. The crystallographic surface texture of the layer is {1, 0, 0}. Cross sections of the layer show that the twin and grain boundaries usually run approximately perpendicular to the substrate, indicating that the layer consists mainly of single layers of crystals.

Material characterization of the layer tends to indicate that the mullite substrate may to some degree be chemically contaminating the silicon coating. This is a problem which must be resolved.

To data photodiodes have been fabricated from state-of-the-art layers, and an analysis of their characteristics indicate that they have an inherent conversion efficiency of approximately 5%.

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SUMMARY

This report covers the work performed under this contract from October 21, 1975, through September 17, 1976. The purpose of the program has been to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by dip-coating inexpensive ceramic substrates with thin layers of polycrystalline silicon. The dip coating methods studied were directed toward a minimum-cost process with the ultimate objective of producing solar cells with a terrestrial conversion efficiency of 10 percent or greater.

The technique for accomplishing the above goal is based on the principle that if a ceramic substrate is coated with a carbon film prior to being immersed into molten silicon the substrate will be wet by the silicon, upon withdrawing it from the melt, to produce a thin (25μm to 100μm) layer of large-grain sheet silicon.

The technique shows promise for excellent low-cost, labor-saving scale-up potentialities and provides an end product of sheet silicon with a rigid and strong supportive backing. A similar supportive backing must be provided for sheet silicon produced by any method. With this method it should be possible to silicon coat several wide, large-area substrates in one dipping operation. The operation could be continued on a 24-hour-per-day schedule by engineering a method for replenishing the silicon melt. An alternative plan would be to coat, in a continuous process, large-area, linked substrates. This research program has been structured to investigate and provide answers regarding the feasibility of the above approach.

An experimental dip-coating facility was designed and constructed to help instrument this investigation. It was constructed with considerable research versatility to study growth parameters necessary for preparing silicon coatings with optimized grain sizes.

The Honeywell Ceramics Center assumed the responsibility for providing the Honeywell Corporate Research Center with the ceramic substrates used in the dip-coating investigation. The Ceramics Center, in addition to purchasing or developing substrate materials, spent some time examining several processing approaches which could be scaled up to square-meter-size substrates. These approaches include rolling, casting, doctor blading and hot pressing. Rolling of a high-plasticity mullite material has been examined, and substrates as large as 500cm^2 have been formed and fired. Rolling and doctor blading of a calcium-aluminate-bound alumina material has also been shown to be feasible. Casting and doctor blading of a silica substrate has also been demonstrated. Hot pressing of fiberglass products into large 500cm^2 sheets has also been accomplished.

Of the numerous ceramic substrate materials dip-coated, a rolled, dried and fired mullite processed by the Ceramic Center has been thus far defined as a candidate for satisfying two of three important criteria for the dip-coating process. Its unique and cost-effective fabrication process is believed to satisfy the long-range economic goals of JPL's Low-Cost Silicon Solar Array Project, and its thermal expansion coefficient is sufficiently compatible with that of silicon.

Ceramic substrates have been successfully dip-coated with silicon having areas as large as 25cm^2. Carbon wafers and sheets of Graphoil (a 4-mil-thick graphite foil made by Union Carbide) have also been successfully dip-coated.

Of the substrate carbonization techniques investigated, a method whereby carbon is physically rubbed over the surface of the substrate has thus far given the best silicon coatings. While generally the silicon coatings have excellent adherence to the substrate, an occasional layer separation prompted an investigation of the bonding mechanism. The carbon films acts as a wetting agent, but the actual silicon-ceramic bond is mechanical in nature, with

silicon penetrating tiny pores in the substrate. The thickness of the carbon film and the porosity of the substrate are parameters which affect the bond.

Crystallization of the coatings occur at the liquid-solid interface at an angle with the substrate that ensures continued nucleation from previously grown silicon. This growth manner provides sheet silicon with single-crystal grains orders of magnitude larger than the sheet layer thickness. Silicon dip-coated layers have been grown with thicknesses from a few microns to as thick as 0.011 inch. Their surface morphology and thickness are dependent upon pull rate and melt temperature. Useful layers 25μm to 75μm in thickness have been produced at pulling rates of 0.1 to 0.15 cm/sec in a melt 5° to 8°C above the melting point of silicon. Layers 50μm thick have single dendritic grains typically 1mm wide tending to extend over the length of the substrate with the long dimension of the dendrite along the pulling direction. The crystallographic surface texture of the layer is {1.0.0}. Cross sections of the layers show that the twin and grain boundaries usually run from the substrate to the surface of the layer indicating that the layer consists mainly of a single layer of crystals.

The silicon coatings are intentionally boron-doped to have a resistivity of 2.5 ohm-cm, p-type. Electrical characterization has shown the resulting layers to have a lower resistivity (0.7 to 2.0 ohm-cm). The lower resistivity has been shown, by IR transmission measurements, to result from additional aluminum acceptor atoms. This aluminum is suspected to originate from slight dissolution of the mullite substrate into the molten silicon. The Hall mobility of the 0.7-ohm-cm layers is about one-half that of single-crystal silicon at 300°K. Higher purity mullite substrates and/or substrate carbon coatings which are impervious to impurity diffusion are being considered to offset contamination from the substrate. Spreading resistance measurements reveal no detectable decrease in electrical conductivity as the probe crosses twin boundaries in the silicon layer.

A diffusion furnace has been set up, and dip-coated layers along with single crystal control samples have been subjected to phosphorus diffusion to produce p-n junctions. To date the optimum junction depth and surface concentrations have not been achieved, but mesa-type photodiodes have been made, and their diode and photovoltaic characteristics have been evaluated. After correcting for their lack of an antireflection coating and their excess series resistance resulting from their fabrication geometry, the dip-coated layers showed an inherent conversion efficiency of approximately 5%.

INTRODUCTION

This report covers the work performed under this contract from October 21, 1975, through September 17, 1976. The purpose of the program has been to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by dip-coating some inexpensive ceramic substrate with a thin layer of polycrystalline silicon. The dip-coating methods studied were directed toward a minimum-cost process with the ultimate objective of producing solar cells with a terrestrial conversion efficiency of 10% or greater.

Previous to the present research program, the Honeywell Corporate Research Center experimentally demonstrated that, if a carbon coating is applied to one face of a ceramic substrate and subsequently dipped into molten silicon, silicon will wet and adhere to only that carbonized face of the substrate. This technique, of course, represents a cost-effective method for producing large areas of sheet silicon with minimal silicon consumption. In addition, the technique shows promise for excellent low-cost labor-saving scale-up potentialities and provides an end product of sheet silicon with a rigid and strong supportive backing. A similar supportive backing must be provided for sheet silicon produced by any method. With this method, it should be possible to silicon coat several wide, large-area substrates in one dipping operation. The operation could be continued on a 24-hour-per-day schedule by engineering a method for replenishing the silicon melt. An alternative plan would be to coat, in a continuous process, large-area linked substrates. This research program has been structured to investigate and provide answers regarding the feasibility of the above approach. To provide such answers the following major tasks must be accomplished:

- Design and construct an experimental dip-coating facility with considerable research versatility to be used to study the growth parameters necessary for preparing silicon coatings with optimized grain sizes.

- Prepare a Standard Operation Procedure document describing the operation of the above dip-coating facility.

- Develop a suitable ceramic substrate which has physical and chemical properties compatible with the dip-coating process.

- Develop a practical and inexpensive method for carbonizing the ceramic substrate.

- Characterize the growth parameters required to produce large-grain, low-dislocation-density silicon coatings in a cost-effective manner.

- Define the physical and chemical properties of a suitable ceramic substrate material.

- Evaluate the physical, chemical and electrical properties of the silicon layers in terms of their solar cell quality potentialities.

- Fabricate solar cells from dip-coated layers of silicon and evaluate them in relation to single-crystal solar cells fabricated under identical conditions.

The balance of this document reports the progress made toward assessing the technical and economic feasibility of the above approach.

TECHNICAL DISCUSSION

EXPERIMENTAL DIP-COATING FACILITY

To systematically perform an investigation of the growth parameters which affect grain size, dislocation density and layer purity, a versatile and reliable experimental facility had been assembled. To the greatest extent possible, the facility was designed and constructed such that its characteristics do not further complicate the problems to be solved. Since modifications were expected from time to time, sufficient design flexibility permit such modifications to be performed with minimum time and expense. To date this flexibility has permitted such modifications. A sectional drawing of the facility is shown in Fig. 1 and a photograph of the assembled facility is shown in Fig. 2. The following research capabilities are included in the present version of this facility:

- An "ultra carbon" silicon melt-heating element powered by a 25-kW SCR-controlled power supply.

  This melt heater is sufficiently overpowered to permit rapid melting of the silicon charge. In addition to saving time, it is generally believed that a cleaner melt surface is attainable by rapid melting procedures. The heating element and power supply were purchased by Honeywell from the Arthur D. Little Co. of Cambridge, Mass. It was designed and constructed to become an integral part of the overall dip-coating facility. The heater assembly is mounted on a water cooled copper base and has only "ultra carbon" cylinders and carbon felt for insulation. While this method of insulation is highly inefficient, it does reduce melt chamber chemical contamination to a minimum.

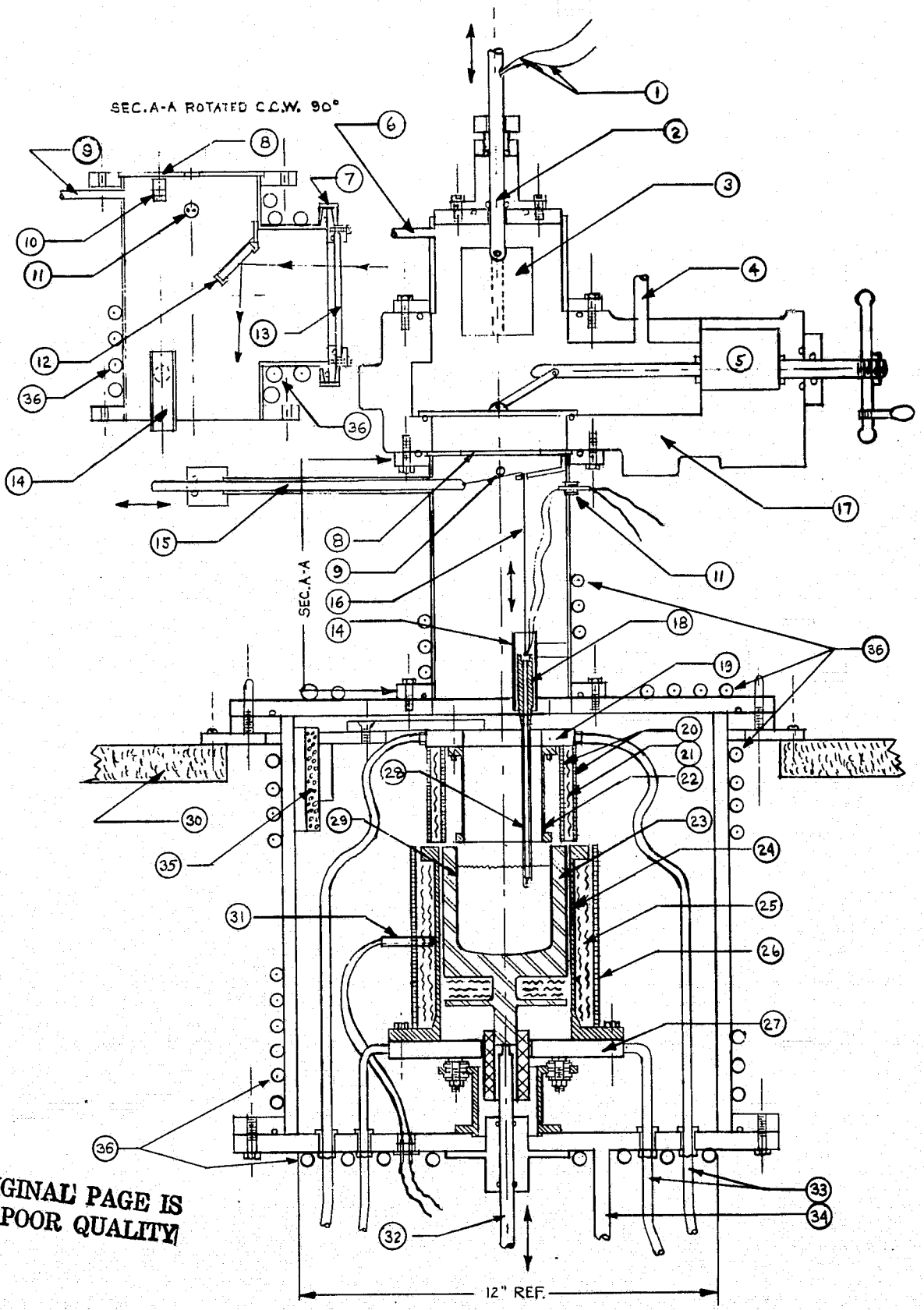


Figure 1a. Experimental Dip-Coating Facility - Sectional View
(See Figure 1b for nomenclature)

(1) Substrate Thermocouple Lead Wires
(2) Dip-Pull Quartz Tube
(3) Ceramic Substrate
(4) Gas Lock Chamber Pumping Port
(5) Gate Valve Gear Box
(6) Gas Lock Chamber Gas Outlet
(7) Vacuum Connector Clamp
(8) Stainless Steel or Moly Heat Shield
(9) Melt-Dipping Chamber Gas Outlet
(10) Melt Thermocouple Wire Guide
(11) Melt Thermocouple Feed-Thru
(12) 45-degree Chromium Plated Mirror
(13) Quartz Window
(14) Melt Thermocouple Weight Guide
(15) Melt Thermocouple Positioning Rod
(16) Nichrome Wire
(17) Vacuum Gate Valve
(18) Melt Thermocouple Weight
(19) Water-Cooled "After Heater" Base Plate
(20) Graphite Heat Shields ("After Heater")
(21) Carbon Felt Insulation ("After Heater")
(22) Graphite "After Heater"
(23) Crucible Holder (Graphite)
(24) Graphite Silicon Melt Heater
(25) Carbon Felt Insulation (Silicon Melt Heater)
(26) Graphite Heat Shield (Silicon Melt Heater)
(27) Water-Cooled Silicon Melt Heater Base Plate
(28) Quartz-Covered Melt Thermocouple
(29) Quartz Crucible
(30) Dip-Coating Facility Main Frame
(31) Silicon Melt Heater Control Thermocouple
(32) Crucible Positioning Rod
(33) Water-Cooled Heater Electrical Leads
(34) Melt-Dipping Chamber Pumping Port
(35) Ceramic Insulation
(36) Water-Cooled Surfaces

Figure 1b. Experimental Dip-Coating Facility - Nomenclature

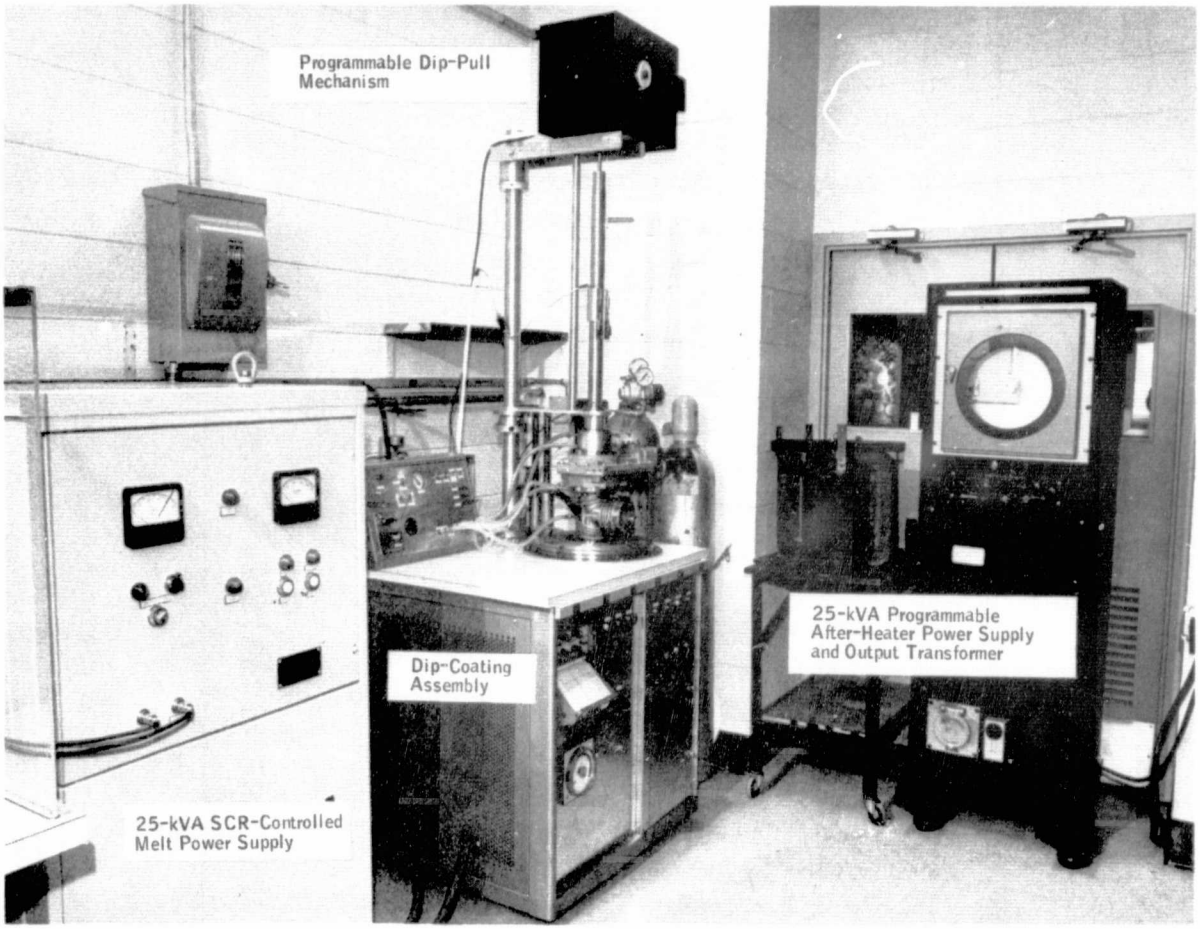


Figure 2. Experimental Dip-Coating Facility Equipment

- Two thermocouples (TC) (Pt - Pt + 13% Rh). One of these is located in the base of the ultra carbon crucial holder. The other may be lowered into the melt once the silicon has become molten (see Fig. 3). The TC located in the base of the crucible holder is used to control the melt heater power supply. The melt TC is shrouded by a replaceable quartz cover of semiconductor purity.

- A Honeywell Dialatrol Temperature Controller.

  The temperature controller feeds a proportioning current to the SCRs in the 25 kW power supply. It does an excellent job of controlling at any given temperature, but, because of its broad temperature range (0°-1600°C), it is impossible to effect a temperature change of less than 3° to 4°C to either direction of temperature.

- A water cooled stainless steel melt chamber and viewing port assembly.

  This water cooling is needed to offset the lack of heater-element insulation. This feature also contributes to a low level of chemical contamination. The cleanable viewing port is used for visually observing the substrate as it is entering and leaving the melt.

- A gas-lock chamber which permits the operator to load uncoated substrates and remove coated ones without shutting down the melt power.

  This feature is made possible by a large vacuum gate valve which is located between the dip-coating chamber and the gas-lock chamber. The gas-lock chamber is readily purged with argon prior to opening the gate valve.

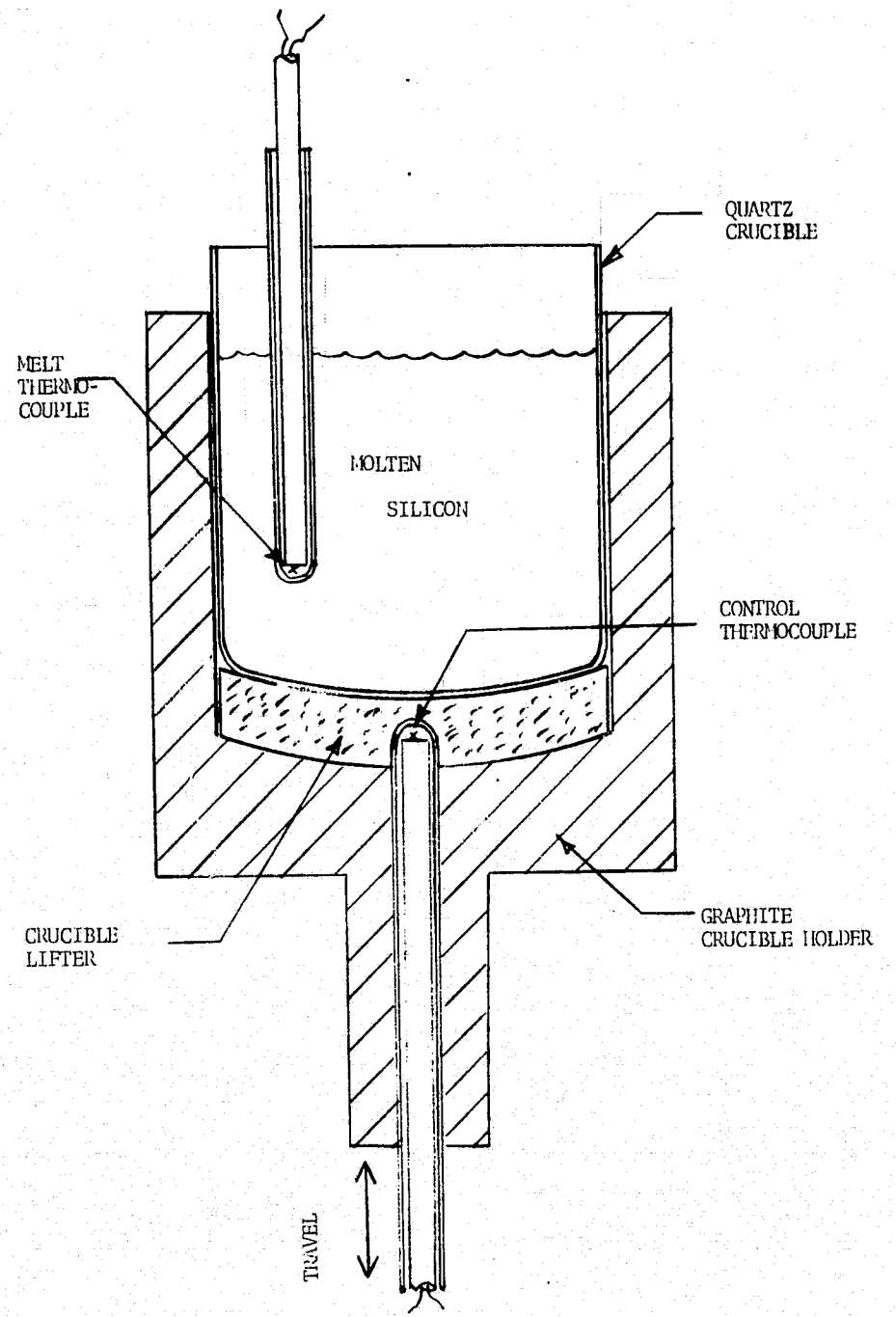


Figure 3. Dip-Coating Facility Thermocouple Configuration (75% of full scale)

- A programmable, variable-speed dipping and pulling mechanism.

  The pulling rate for satisfactory coatings is melt-temperature dependent and thus must be variable. A high degree of nucleation from previously grown silicon occurs as the substrate is being withdrawn from the melt. Therefore, it is beneficial to have the capability of programming the pulling rate such that, as the substrate emerges from the melt, the pulling rate is increased by an amount corresponding to the crystalline grain development. This feature is accomplished by a programmable cam on the dipping and pulling mechanism.

- A two-pen Honeywell electronic-type chart recorder for recording of the substrate position and temperature, both with reference to the surface of the melt.

  To efficiently characterize the optimum growth parameters, it is mandatory that the growth conditions be accurately recorded for each sample substrate that is dip-coated. By doing so, as the physical properties of each coated sample are analyzed with respect to their particular growth conditions, positive direction can be given to the investigation. To accomplish this capability, the dipping and pulling mechanism is designed to provide an electrical readout which, when combined with the recorder's chart speed, provides dip-pull rate information.

- An after-heater, if so desired, located immediately above the silicon melt.

  This research capability could increase control of the solidification process and promote continued grain growth as

the substrate is pulled through this regulated temperature zone. Further, by elevating the temperature above the melt, those ceramic substrates more susceptible to thermal shock will be preheated prior to their immersion into the molten silicon. The after heater is powered by a 30kVA stepdown transformer which is controlled by a Honeywell Electrodyne motor-driven multiple variac power supply. The temperature is controlled by a programmable cam controller with a circular chart recorder.

- A capability for orienting the substrate at an angle while performing the dip-pull operation.

  To date, there are no well-defined theories which suggest angle dipping may enhance grain size, but intuitively one expects that dipping an angle-oriented substrate would certainly modify the liquid-solid interface, perhaps in a beneficial way. Therefore, should this later be considered a desirable feature, provisions for this capability are designed into the facility.

- Two adjustable gas flowmeters, one for regulating and monitoring the gas flow through the melt chamber and another for purging the gas lock assembly.

- A two-way gas valve for transferring from one argon gas cylinder to another should a high purity of argon be desirable during a particular stage of the dip-coating cycle.

- A water failure shutdown switch

- A control panel for operating the facility

CERAMIC SUBSTRATE PROCUREMENT AND DEVELOPMENT

The Honeywell Ceramics Center has assumed the responsibility for providing the Honeywell Corporate Research Center with the ceramic substrates used to date in the dip-coating investigation. The Ceramics Center, in addition to purchasing or developing substrate materials, spent some time examining several processing approaches, which could be scaled up to produce square-meter-size substrates. These approaches include rolling, casting, doctor blading and hot pressing. Rolling of a high plasticity, mullite material has been examined and substrates as large as 500cm^2 have been formed and fired. Rolling and doctor blading of a calcium aluminate bound alumina material has also been shown to be feasible. Casting and doctor blading of a silica substrate has also been demonstrated. Hot pressing of fiberglass products into large 500cm^2 sheets has also been accomplished.

Standard 25cm^2 test samples for this program were prepared or received from vendors as indicated in Table 1. Each of these materials is discussed in the following paragraphs.

Mullite

Mullite is an aluminum silicate compound ($3Al_2O_3 \cdot 2SiO_2$) which is available in many forms. The crystalline material has a melting point of about 1850°C, but up to 30% glassy phase is commonly found in this material which lowers the softening temperature. The thermal expansion and conductivity of mullite is about 5.0×10^{-6}/°C and 3.5 Btu/hr-ft°F, respectively, and its theoretical density is 3.26 gm/cc. The following four types of mullite were obtained for this program.

- Honeywell rolled MV-20
- McDanel cast MV-30

Table 1. Substrate Materials Investigated

Material	Trade Name	Source	Fabrication Process	Firing Temperature
Mullite	MV-20	McDanel Corp.	Rolling	1640°C 20% glass
Mullite	MV-30	McDanel Corp.	Casting	-- 15% glass
Mullite	Fiberfrax	Carborundum	Hot pressing	1400°C
Mullite		American Lava	Pressed	
Cordierite	Alsimag 701	American Lava	(purchased)	--
Cordierite	A-3171	Du-Co	(samples)	--
Alumina	Alsimag 614	American Lava	(purchased)	-- 96% Al_2O_3
Alumina	Alsimag 798	American Lava	(purchased)	-- 85% Al_2O_3
Polygranular SiO_2	GP-31	Glasrock Products, Inc.	Casting	1160°C 1400°C 1640°C
Calcium Aluminate	CA-25	Alcoa	Pressing and rolling	60°C 1160°C 1640°C
Zirconia	Alsimag 475	American Lava		
Sapphire	To be acquired			

- Honeywell hot-pressed Fiberfrax
- American Lava pressed material

McDanel mullite composition MV-20 was procured in a plastic extrudable form. Test substrates (2 x 2-1/2 x 1/16 inch thick) were produced by rolling the material over a smooth, oiled surface and controlled drying and firing to 1640°C. After rolling, the sheet material was cut to oversized (2-1/4 x 3-3/4 inch) coupons. The coupons were dried between flat plaster of Paris blocks for 20 hours at 60°C. They were then bisque fired on mullite sagger plates to 600°C and finally high-temperature fired (on mullite) to 1640°C. The slight warpage which occurred during high temperature firing is attributed to non-uniform heating in the high convection gas-fired kiln. A total of 38, 2 x 2-1/2-inch substrates have been produced. Several larger 3 x 5-inch substrates and 8 x 9-inch substrates were successfully prepared of this material by the rolling methods.

A second McDanel mullite composition, MV-30, was procured in fired tubular form. Eight (2 x 2-1/2 x 3/16-inch thick) test coupons were cut from this material. The MV-20 and MV-30 materials typically contain 20 and 15% glassy phase after firing, respectively.

An additional 100 2 x 2 x 0.1-inch experimental pressed mullite substrates were received from American Lava Division of 3M Inc. Rigid sheets of mullite fibers have also been formed by pressing double or triple layers of Fiberfrax (0.05-inch-thick Carborundum sheet) under a load at 1400°C. Flat, very porous, rigid sheets 0.04 to 0.06 inch thick with a density of 0.5 gm/cc were formed by this process.

Alumina

Alumina substrates are the most common type of flat ceramic material used for electronic circuitry. Pure Al_2O_3 has a melting point of about 2000°C and a thermal expansion and conductivity of 6.7° to 10^{-6}/°C and 10.0 Btu/hr-ft-°F, respectively. The theoretical density of this material is 3.98 gm/cc.

Two types of alumina substrates were obtained for this program. One-hundred pressed 96% and 85% alumina 2 x 2 x 0.05-inch plates were procured from American Lava. These are designated as Alsimag 614 and 798, respectively. A third type of alumina was fabricated at Honeywell by rolling, pressing and doctor blading a calcium-aluminate-bound alumina material. Table 2 gives four compositions that were formulated from Alcoa CA-25 calcium aluminate cement and tabular alumina filler. The consistency of the mixture was varied by addition of water based on the method of forming.

Smooth compress surfaces with no sticking were accomplished at 5000-psi pressure. No apparent warpage occurred during firing. Rolled substrates had some surface roughness, and slight warpage occurred during high-temperature firing. These materials were still somewhat porous but still had a density over 3.0 gm/cc.

Zircon

Zircon is a zirconia silicate ($ZrO_2 \cdot SiO_2$) compound with a melting point of 1530°C and theoretical density of 4.68 gm/cc. The thermal expansion and conductivity of this material is 6.0 x 10^{-6}°C and 3.8 Btu/hr-ft-°F, respectively.

Table 2. Honeywell Ceramics Center Formulation Data

Formulation No.	Materials	Proportions (% by wt)	Water (% by wt)	Forming Methods	Drying (60°C)	Bisque Firing (600°C)	H.T. Firing (1160°C)	H.T. Firing (1400°C)	H.T. Firing (1640°C)
1	Alcoa CA-25 Tab. Al_2O_3-325 Tab. Al_2O_3-48	55 30	20	Casting	X				
2	Glasrock GP-31	100	20	Casting	X X	X X	X	X	
3	Glasrock GP-31 Glasrock GP-71	80 20	19	Casting	X X	X X	X		X
4	Alcoa CA-25 Tab. Al_2O_3-325	15 85	10	Pressing	X	X	X		
5	Alcoa CA-25 Tab. Al_2O_3-325 Tab. Al_2O_3-48	15 70 15	12	Pressing	X	X	X		
6	Alcoa CA-25 Tab. Al_2O_3-325 Tab. Al_2O_3-48	15 55 30	10 15 1/2	Pressing Rolling	X X X X	X X X X	X X		 X X
7	Carborundum Fiberfrax			H.T. Sinter				X	

Cordierite

Cordierite is a magnesium aluminum silicate ($2M_5O \cdot 2Al_2O_3 \cdot 5SiO_2$) with a melting point of 1200°C; however, slightly different modifications may be as high as 1400°C. This material has a thermal expansion of 1.5×10^{-6}/°C.

Sample Cordierite substrates were obtained from the following two suppliers:

- Minnesota Mining and Manufacturing Co. (3M - Alsimag 701)
- Du-Co Ceramics Co. (A-3171)

A specimen of each material was fired at 1500°C with the results shown in Fig. 4. Both materials show leaching out of a lower-melting-point constituent. The 3M material retains its shape, but the Du-Co material melted completely. The Du-Co material was therefore not evaluated for the silicon dip-coating application.

Silica

Silica in powdered form was procured from Glasrock Products. This Glasrock grade "I" material (99% SiO_2) was of two particle sizes designated GP31 (Fisher sieve 2.0) and GP71 (Fisher sieve 4.5).

Two formulations were made (see Table 2). In each case, a slip was prepared by high-shear mixing of the solid ingredients and water. The material was then cast on a flat porous substrate. The castings were dried at 60°C, bisque fired at 600°C, and subsequently high-temperature fired at either of two higher temperatures (see Table 1).

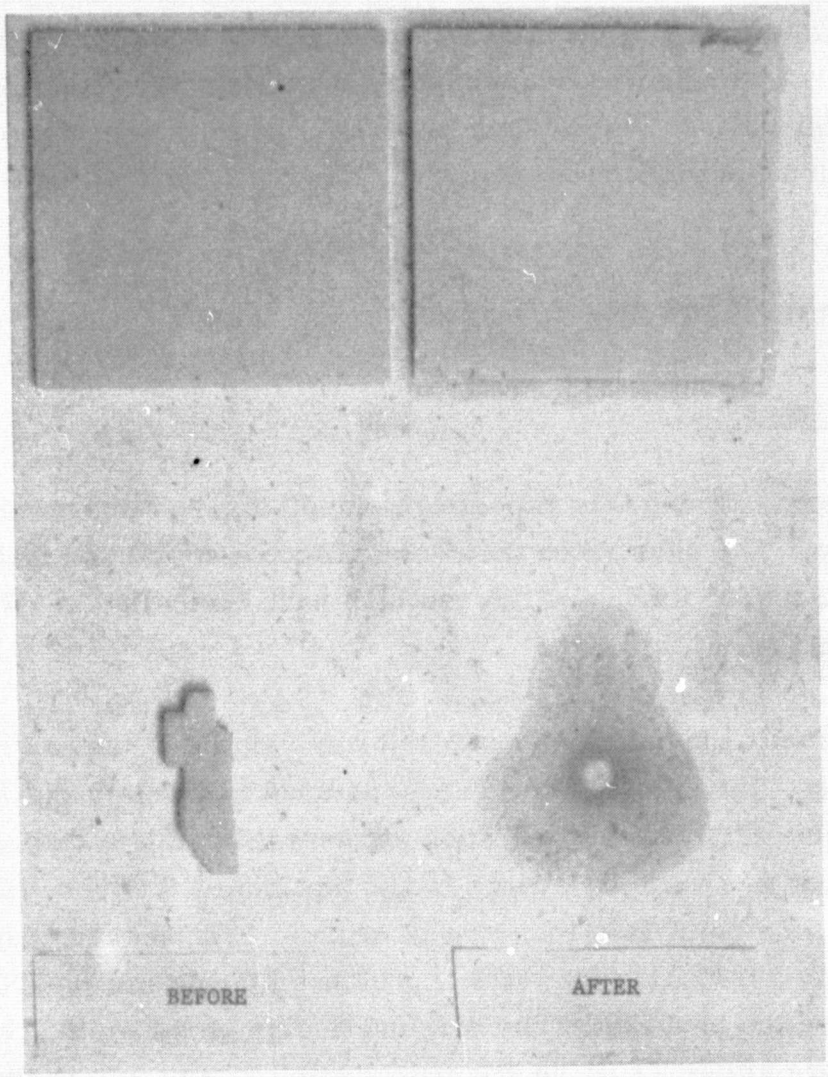


Figure 4. Cordierite Substrate Samples – 3M Alsimag 701 (top) and Du-Co A3171 – Before and After Firing at 1500°C

A slight warpage of the cast sheets occurred after high-temperature firing. This is attributed to a nonuniform particle size distribution through the sheet thickness. The fired substrates appear to have adequate structural strength for subsequent processing.

DIP-COATING RESULTS

General Discussion

In general, during this reporting period, dip-coating results have been encouraging. The substrates that were silicon coated have mainly been sized to 2-1/2 x 2 x 0.05 inch, and the coatings have typically been 20 to 25 cm^2 in area (see Fig. 5).

The principal problem encountered was related to measurement of the melt temperature. Initially mullite tubing was used to insulate the Pt - Pt + 13% Rh thermocouples (TC), and it was soon determined by an EDAX analysis that the mullite tubing was yielding silicon to the platinum TC wires, thus forming an eutectic melting point less than that of silicon. The thermocouple tubing was replaced with 99.8% alumina, which prolonged the life of the TCs but by no means solved the problem. The original design of the melt TC and control TC did not isolate either TC from the silicon-rich vapors within the melt chamber. For this reason the TCs would not only drift in their calibrated output but eventually combined with enough silicon to once again fail. The problem was corrected for the control TC as shown in the before and after drawings of Fig. 6. Note that, initially, the melt chamber was sealed off by an O-ring surrounding the alumina TC tube. After the modification, the chamber was sealed off by an O-ring which surrounds a sealed alumina tube which covers the TC tube, thereby isolating it from the melt chamber environment. Unfortunately, no realistic solution has been devised for isolating the melt TC from the surrounding silicon vapors. Therefore, the more recent melt temperatures reported are referenced to the indicated temperature where silicon solidification is first observed in the melt.

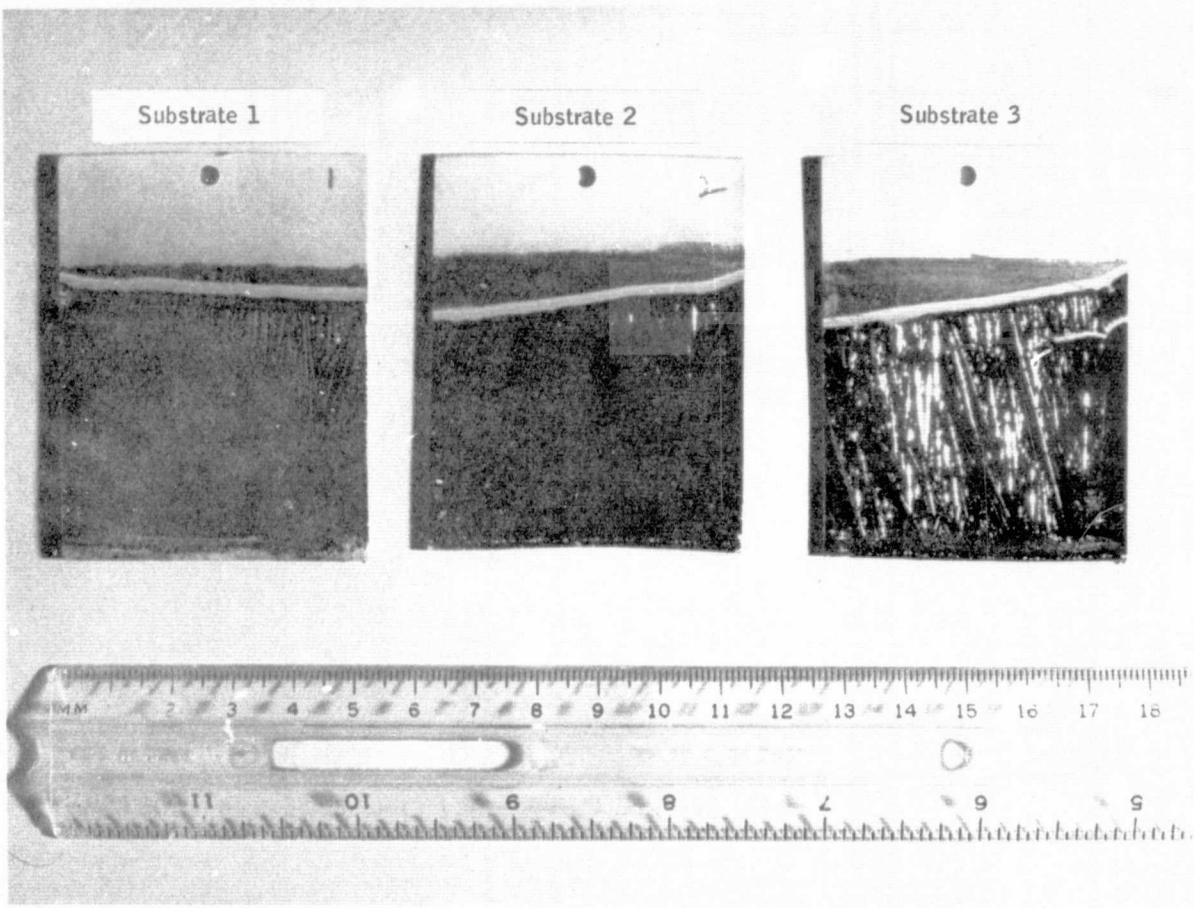


Figure 5. Dip-Coated Substrates

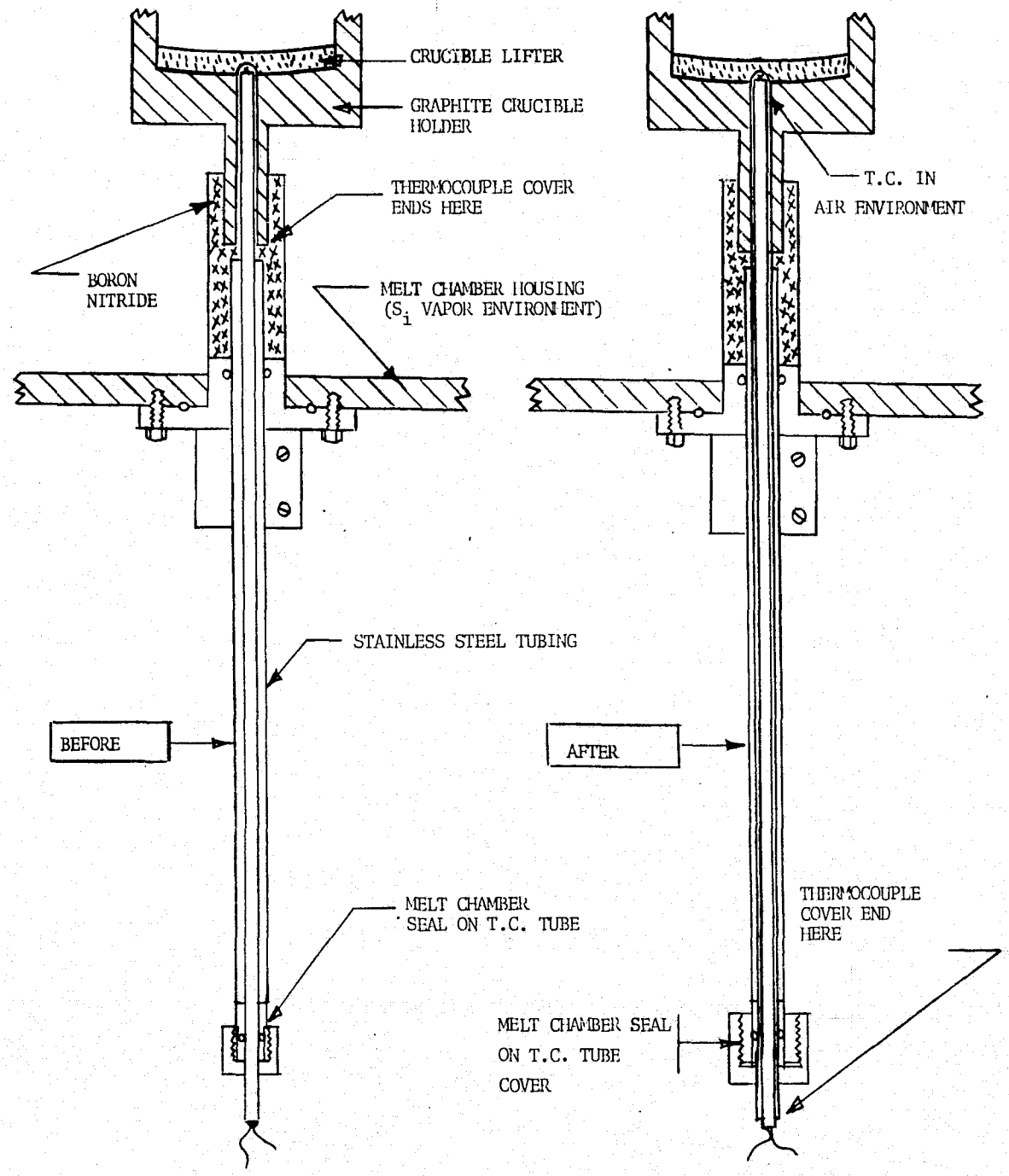


Figure 6. Control Thermocouple Modification

Substrate Characterization

With the exception of the cordierite substrate, all of the ceramics previously discussed have been dip-coated with varying degrees of success. Table 3 lists this variety of substrates along with carbon and Graphoil substrates. All of the materials listed, with the exception of American Lava's pressed mullite, withstood the thermal shock of being immersed into molten silicon with only a relatively short preheat cycle prior to their immersions. Of those listed, the McDanel MV-20 mullite plastic composition, which was rolled, dried and fired at 1640°C by Honeywell's Ceramics Center, stands out as a strong favorite at this time. This ceramic, as a substrate, has already been shown to satisfy two of three important criteria for being defined as a suitable candidate for the dip-coating process. Its unique and cost-effective fabrication process is believed to satisfy the long-range economic goals of JPL's Low-Cost Silicon Solar Array Project, and its thermal expansion coefficient (5.0×10^{-6}°C) is sufficiently compatible with that of silicon. No obvious stress or strain has been evident, to date, in either the silicon coating or the substrate. The third important criterion, which this form of mullite must satisfy, is the extent to which its chemical composition will influence the purity of the silicon coated upon it. This criterion is still being investigated. Surprisingly, near the end of this reporting period, the pressed mullite substrates procured from the American Lava Co. have not consistently withstood the thermal shock of being immersed into molten silicon, nor do they display a thermal expansion coefficient compatible with that of silicon. This was manifested by the degree of cracking observed in those substrates which survived the dip-coating process. So different, in fact, is their behavior from the McDanel MV-30 rolled, dried and fired mullite that suspicion arose as to whether they were actually mullite. A diffraction analysis was performed on a sample of this pressed mullite, and the data was compared against that of the ASTM Powder Diffraction File. It was confirmed that they were mullite. Their different behavior is not yet understood, but the Ceramics Center suggests they may possess a different percentage of glassy phase from that of the MV-20 composition. The Ceramics Center is consulting with American Lava to resolve this difference.

Table 3. Summary of Dip-Coated Substrates

Substrate No.	Run No.	Substrate Material	Pulling Rate (cm/sec)	Melt Temperature (°C)	Layer Thickness (μm)	Layer Ave ρ (ohm-cm)
MR-1	7	Mullite[a]	0.12	1434	45	1.8
MR-2	7		0.33	1426	8-10	0.49
MR-3	7		0.33	1410	15-125[b]	0.7
MR-4	8		0.1	TCF[c]	~ 15	0.64
MR-5	8		0.1	TCF[c]	Given to JPL	
MR-5A	8		0.1	Substrate froze in melt		
MR-6	9		0.35	TCF[c]	~ 8	0.77
MR-7	9		0.284	TCF[c]	32-37	0.82
MR-8	10		0.233	1411	25-38	1.34
MR-9	10		0.1	1426	50	0.52
MR-10	11		0.155	1436	10	0.047
MR-11	11		0.086	1436	45	0.47
MR-12	11		0.054	1455-1457	25-37.5	1.7
MR-13	11		0.064	1412	279	1.12
MR-14	11		0.084	1439	~ 30	0.9
MR-15	12		0.17	1441	NM	NM
MR-16	12		0.085	1448	~ 25	0.9
MR-17	13		0.104	1433	NM	NM
MR-18	13		0.0933	1437	NM	NM
A95-1	7	Alumina[d]	0.1	1444	~125	4.6
A95-2	9	Alumina[d]	0.1	TCF[c]	Substrate shattered	
A85-1	10	Alumina[e]	0.175	1419	~50	NM
Z-1	12	See Note[f]	0.085	1437	NM	NM
CA-1	12	See Note[g]	0.097	1437	NM	NM
FF-1	13	See Note[h]	0.117	1456	NM	NM
C-1	9	Carbon	0.109	TCF[c]	NM	NM
C-2	10	Carbon	Broke in silicon melt			
C-3	10	Carbon	0.175	1416	NM	NM
G-1	11	"Graphoil"	0.175	1439	NM	NM

[a] McDanel MV-20 rolled, dried and fired
[b] Dendrites protrude above surface
[c] Thermocouples failed
[d] 96% Alumina
[e] 85% Alumina
[f] Zircon (Zirconia sillicate - $ZrO_2 \cdot S_iO_2$)
[g] Calcium Aluminate-bound Alumina
[h] Carborumdum pressed Fiberfrax

NM = not measured

Table 3. Summary of Dip-Coated Substrates (Concluded)

Substrate No.	Run No.	Substrate Material	Pulling Rate (cm/sec)	Melt Temperature (°C)	Layer Thickness (μm)	Layer Ave ρ (ohm-cm)
MR-19	15	Mullite[a]	0.1	1427	20	NM
MR-20	15		0.2	1423	10	NM
MR-21	15		0.3	1419	10	NM
MR-22	15		0.4	1417	10	NM
MR-23	15		0.085	1418	NM	NM
MR-24	17		0.1	~1445	25	NM
MR-25	17		0.2	~1445	5-10	NM
MR-26	17		0.3	~1445	12	NM
MR-27	22		0.094	1443	12	NM
MR-28	22		0.09	1421	25-150	NM
MR-29	22		0.043	1422	12-30	NM
MR-30	22		0.09	1425.5	25-150	NM
MR-31	22		0.31	1427.5	12-20	NM
MR-32	22		0.06	1430	~100	NM
MR-33	22		0.06	1428	90-150	NM
MR-34	22		0.085	1433	50-125	NM
MR-35	23		0.1	1423	25-50	NM
MR-36	23		0.21	1423.5	12-15	NM
MR-37	23		0.1	1420	25-125	NM
MR-38	23		0.1	1422	12-40	NM
MR-39	23		0.1	1420.5	12-20	NM
MR-40	23		0.2	1420.5	12-20	NM
MP-1	21	Pressed[b] Mullite	Substrate shattered upon dipping			
MP-2	21	Pressed[b] Mullite	Substrate shattered in melt			
MP-3	22	Pressed[b] Mullite	0.7	1433	NM	NM
PS_iO_2-1	23	Polygranular Silica	0.085	1421	NM	NM

[a]McDanel MV-20 rolled, dried and fired

[b]American Lava (3M Co.)

Of the two types of alumina substrates listed, namely: 96% and 85% alumina, the 96% alumina appears least likely to accommodate the dip-coating process. The 96% alumina has a thermal expansion coefficient of about 6.7 x 10^{-6}/°C, which represents a rather substantial mismatch with silicon. The 96% alumina substrate A95-1 was dip-coated without a routine substrate cleaning process for the purpose of testing its resistance to thermal shock. Because of the uncleanness of its surface, only a spotty silicon coating was achieved. In this case, no visible signs of cracking took place. The 96% alumina substrate A95-2, on the other hand, was cleaned and fired prior to dip-coating it with silicon. The dip-coating exercise produced a smooth 100μm-thick layer as viewed through the viewing port of the dip-coating facility. This layer, however, prior to being removed from the dip-coating facility, shattered upon cooling, apparently because of its thermal expansion mismatch with silicon. Prior to this contract program, a much thinner (~15μm) silicon coating was successfully placed on a high-purity alumina substrate; therefore, 96% alumina, at this time, cannot yet be ruled out as a possible substrate candidate. Even though it may be possible to apply a thinner coating, or thicker coating for that matter, and keep the substrate intact by a controlled cooling cycle, the evidence remains that the resulting silicon coatings are likely to be highly stressed. This stress is likely to introduce excessive dislocations with the silicon.

An approximately 50μm silicon coating was placed on an 85% alumina substrate, and this substrate remained intact. Even though 85% alumina has a somewhat smaller thermal expansion coefficient than 96% alumina, there was still evidence of the silicon layer being strained. At the top of the substrate, larger dendrites protruded above the main surface coating. As the substrate continued to be pulled from the melt, a smoother coating was produced, possibly due to the change in heat flow or melt temperature. It was observed that tiny chips of silicon flaked off of these protruding dendrites. This is probably evidence of thermal stress in the silicon. The existence of larger dendrites protruding from the surface followed by a smooth coating is

not unique to this 85% alumina substrate. It has also happened under similar growth conditions with mullite substrates, but portions of the larger dendrites never flaked off as they did on substrate A85-1.

Zircon substrate Z-1 is a zirconia silicate ($ZrO_2 \cdot SiO_2$) compound with a melting point of 1530°C and a thermal expansion coefficient of 6.0×10^{-6}/°C. The silicon coating applied to this substrate also manifested a thermal expansion mismatch by having portions of the silicon coating flake off. There was no observable cracking in the substrate itself, but small (~0.5mm) blisters formed on both sides of the substrate. In spite of these blisters, rather large 1mm x 2cm grains were observed, with the longer dimension, as usual, being aligned along the direction of growth.

Substrate CA-1 is a calcium aluminate-bound alumina. The silicon coating adhered very poorly to this substrate. In addition to having large portions of the layer flake off, several cracks occurred in the substrate. On the basis of one coated substrate, this material would have to be rated as a poor candidate with respect to its compatibility with the dip-coating process.

Substrate FF-1 was fabricated by the Honeywell Ceramics Center from Carborundum Fiberfrax, which is made up of mullite fibers. Sheets from which the above 2-1/2 x 2-inch substrate was cut were formed by hot-pressing (1400°C) double or triple layers of Fiberfrax (0.05-inch-thick carborundum sheet). Flat, very porous but rigid sheets, 0.04 to 0.06 inch thick, with a density of 0.5 gm/cm^3 were formed by this process.

The typical carbon coating technique of rubbing or scrubbing ultrapure carbon over one surface could not be used for this substrate due to its softness. Therefore, high-purity carbon powder was poured on one surface and worked into the pores by rubbing the surface with a clean cloth. The results of the dip-coating process were somewhat surprising. Silicon did not coat the face of the substrate on which the carbon powder was applied, but, oddly,

a very thin coating of silicon occurred on the opposite face. Whether the silicon was wetted by the carbon and subsequently passed through the porous substrate to the opposite face by some wicking action or whether silicon will wet pressed-mullite fibers without the aid of carbon is not known at this time.

Substrate $PSiO_2$-1 is a polygranular SiO_2 fabricated by the Honeywell Ceramics Center as described in the "Ceramic Procurement and Development" subsection. The casting process left the surface of the substrate quite rough and difficult to carbonize by the carbon rubbing technique. The substrate withstood the thermal shock and the high temperature associated with the dipping into molten silicon. In spite of its rough surface texture, a relatively uniform silicon coating was achieved. The backside of the substrate was covered with tiny droplets of solidified silicon which had the appearance of seeping through from the silicon-coated face. SiO_2 itself may, however, be to a limited extent wet by molten silicon. Additional warpage occurred in the dip-coated substrate probably to accommodate for the large thermal expansion mismatch.

Substrates C-1, C-2 and C-3 were machined from high-density carbon to the dimensions of 2-1/2 x 2 x 0.015 inch. The crystalline structure observed on substrate C-1 differed from the usual narrow, long-dendritic-type structure observed on all the ceramic-backed coatings. This, as suggested by Dr. Martin Leipold of JPL, may result from the larger thermal conductivity of carbon as opposed to ceramic materials. This increased thermal conductivity could alter the heat flow pattern that customarily occurs with ceramic substrates.

Substrate C-2 cracked upon being immersed into the melt, and pieces of the carbon initially floated on the surface of the melt. It is interesting to note that, in a time frame of 2 to 3 minutes, these pieces of carbon were either dissolved into the silicon solution or were completely converted to SiC and sank to the bottom of the melt. In any case, if thin wafers of carbon were to be considered as a substrate material for the dip-coating process, further consideration would have to be given to the length of time one is allowed to dip and pull from the melt.

Substrate C-3 was given to JPL prior to any analysis.

A 5 x 2-inch piece of 5-mil Graphoil was wrapped around a 2-1/2 x 2 x 0.05-inch mullite substrate and dip-coated with silicon. It was designated as substrate G-1. Graphoil, a product of Union Carbide, is a graphite foil that can be purchased in a number of thicknesses. Substrate G-1 was dipped and pulled from the melt, allowing no soaking time in the melt. A thin coating of silicon occurred only on the exposed surfaces; unlike carbon substrate C-1, G-1 had long, narrow crystalline grains which were dendritic by nature and very similar to the size and type one would expect on a ceramic substrate coated under similar conditions.

Solidification Conditions Parameters Study

In an effort to determine the influence of pulling rate and melt temperature on the thickness of the silicon coating, 21 samples were dipped under specified conditions where the temperature ranged from 1417°C to 1445°C and the pull rate from 0.06 to 0.4 cm/sec. The growth conditions and coating thicknesses for each sample are provided in Table 4. The larger of the two thicknesses is that of the primary dendrites in the coating.

However, due to the aforementioned problems with the thermocouples used to measure melt temperature and the limitations of the furnace's controller in making it possible to set a desired temperature, given temperatures were difficult to achieve and reproduce. Within the range of scatter, the results then are only qualitative and what would be expected; namely, the higher the melt temperature and the faster the pull rate, the thinner the silicon coating formed. It is not possible at this time to say which, if either, parameter has more influence on thickness than the other.

Table 4. Melt Temperature and Pull Rate Thickness Study

Run No.	Sub No.	Melt Temp. (°C)	Pulling Rate (cm/sec)	Layer Thickness (μm)	Soak Time (sec)
15	MR-19	1427	0.1	20	60
15	MR-20	1423	0.2	10	60
15	MR-21	1419	0.3	10	60
15	MR-22	1417	0.4	10	60
17	MR-24	~1445	0.1	25	?
17	MR-25	~1445	0.2	5.0-10.0	~12
17	MR-26	~1445	0.3	12	60
22	MR-27 1a	1443	0.094	12	50
22	MR-28 2a	1421	0.09	25-150	54
22	MR-29 3a	1422	0.2	12-30	72
22	MR-30 4a	1427.5	0.09	25-150	251
22	MR-31 5a	1427.5	0.31	12-20	50
22	MR-32 6a	1430	0.06	Flaked off	17.5
22	MR-33 7a	1428	0.06	90-150 Flaked off	29
22	MR-34 8a	1433	0.085	50-125 Flaked off	32
23	MR-35 1b	1423	0.1	25-50	110
23	MR-36 2b	1423.5	0.21	12-15	120
23	MR-37 3b	1420	0.1	25-125	60
23	MR-38 4b	1422	0.1	12-40	120
23	MR-39 5b	1420.5	0.1	12-20	158
23	MR-40 6b	1420.5	0.2	12-20	115

SUBSTRATE CARBONIZATION AND SILICON-CERAMIC BONDING

The key to successfully dip-coating various ceramic substrates with silicon is to apply a carbon coating to the surface of the substrate to be coated.

During this reporting period the following methods were explored:

- Rubbing ultrapure carbon over one surface of the substrate with a scrubbing action.
- Applying carbon soot to one surface of the substrate, using an acetylene torch.
- Applying black Aqua-Dag to one surface of the substrate and subsequently firing it at 900°C in an argon atmosphere.
- Applying a liquid coating of pure acrylic [which had been dissolved in 1-2 Dichloroethane ($C_2H_4Cl_2$)] to one surface of the substrate followed by a 900°C firing in an argon atmosphere.
- Pyrolyzing a layer of transparent 3M-brand Scotch tape in a 900°C furnace having a nitrogen atmosphere.

Of the above listed methods, only the rubbed carbon technique has produced uniform coatings of silicon. Except for the Aqua-Dag which flaked off the substrate following the 900°C firing, the remaining methods produced only spotty wetting of the silicon.

Initially it was assumed that the silicon reacted with the carbon to form a thin silicon-carbide (SiC) film which subsequently wet the silicon. It was further presumed that this thin SiC film penetrated the pores of the ceramic

to form a mechanical bond. Occasional layer separation from the ceramic substrate prompted a further study of this silicon-substrate bonding mechanism.

It was observed that, if a very thorough and heavy carbonization was applied to the substrate, thicker (125μm to 250μm) layers will sometimes flake off if the total time the substrate remains in the melt is short. This conclusion is further supported by the fact that the flaking occurs more predominantly near the top of the substrate (that portion which remains in the melt the least time). Visual microscopic examination of the bottom surface of separated layers along with examination of that portion of the substrate from which it separated, strongly suggests that the formation of SiC, if any, plays an insignificant role in bonding the silicon layers to the substrate.

The University of Minnesota is presently performing a Scanning Auger Microscope study on angle-lapped and separated layers which should enlarge upon this visual inspection. One could conclude from the visual inspection, however, that silicon bonds directly to the pores of the ceramic only in regions where there are voids in the carbon coating. These voids could occur partially by an incomplete carbon coating and partially by the thinner regions of the carbon coating entering the silicon solution upon dipping. From the beginning it was observed that, when the substrate was dipped approximately 1/8 inch into the melt and allowed to remain there for a prolonged time, this portion of the substrate had a poor silicon coating. This small portion of the silicon-coated substrate also has a distinct absence of carbon remaining. The possibility exists that at this high temperature there is sufficient oxygen present from the disintegrating quartz crucible to permit carbon monoxide to form, but it is also possible that the carbon is merely going into the silicon solution.

A review of past-coated substrates reveals that layers which have separated from the substrate all remained in the melt relatively short periods of time. On the other hand, if the carbon coating is too thin, as was the case

with the pyrolyzed carbon coatings, the entire carbon film can be dissolved before the silicon can intermittently wet and bond to the substrate, thus producing only spotty wetting. This condition prevailed, however, using a dip-coating cycle which typically produces satisfactory silicon coatings on substrates that were carbonized by the "rubbing" technique. Perhaps by shortening the time the substrate is typically allowed to soak in the melt, these thinner pyrolyzed carbon films may adequately wet the silicon. While the presence of a carbon coating is essential to producing a silicon coating on a ceramic substrate, it appears to act merely as a wetting agent. The exact mechanism is not yet understood.

Figure 7 shows the silicon-ceramic interface of substrate MR-8, unetched. The silicon-ceramic bond is apparently mechanical in nature, formed when the molten silicon penetrates the porous substrate. This intimate contact is achieved over less than 10% of the surface but is generally sufficient to provide excellent adherence of the film to the substrate. The black areas between the silicon and ceramic are believed to be holes where unreacted carbon was pulled out during polishing. Figure 8 shows photographs of the back side of a portion of a separated silicon layer and that portion of the substrate from which it separated. These photographs further illustrate that the silicon bonds directly to the substrate only in regions that are void of the carbon coating.

Figure 9 shows photographs of silicon-alumina and silicon-pressed mullite interfaces, respectively, where the ceramics are not as porous as the rolled mullite and not penetrated by the molten silicon. It was noted that the silicon coating did not adhere as well to these denser ceramics as it did to the more porous rolled mullite. However, it was also noted that, if an exceptionally heavy carbon coating is supplied to the rolled mullite, the silicon does not adhere well to it either.

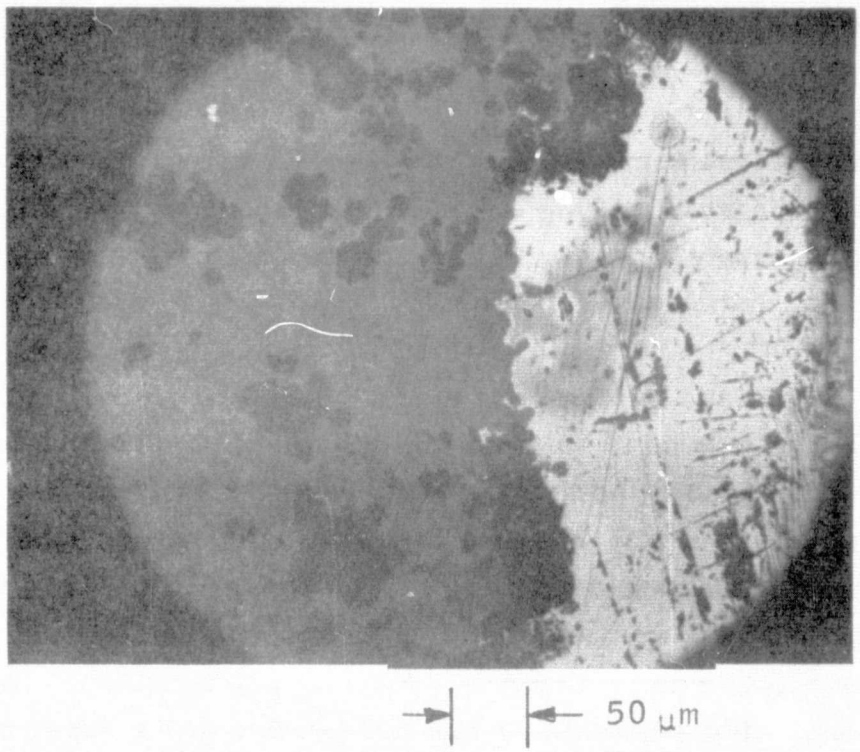
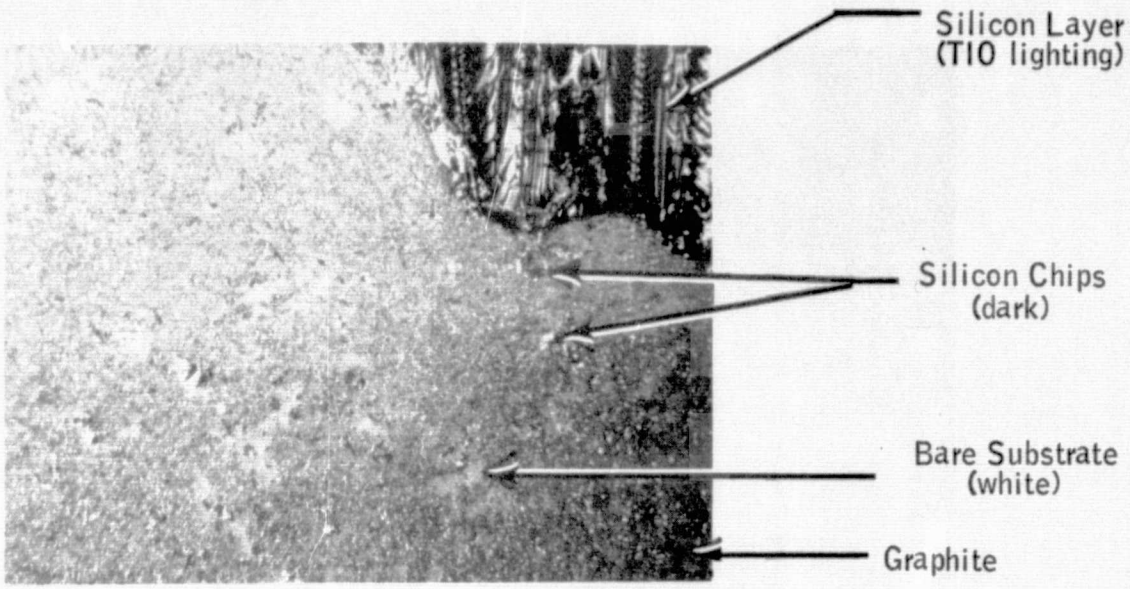
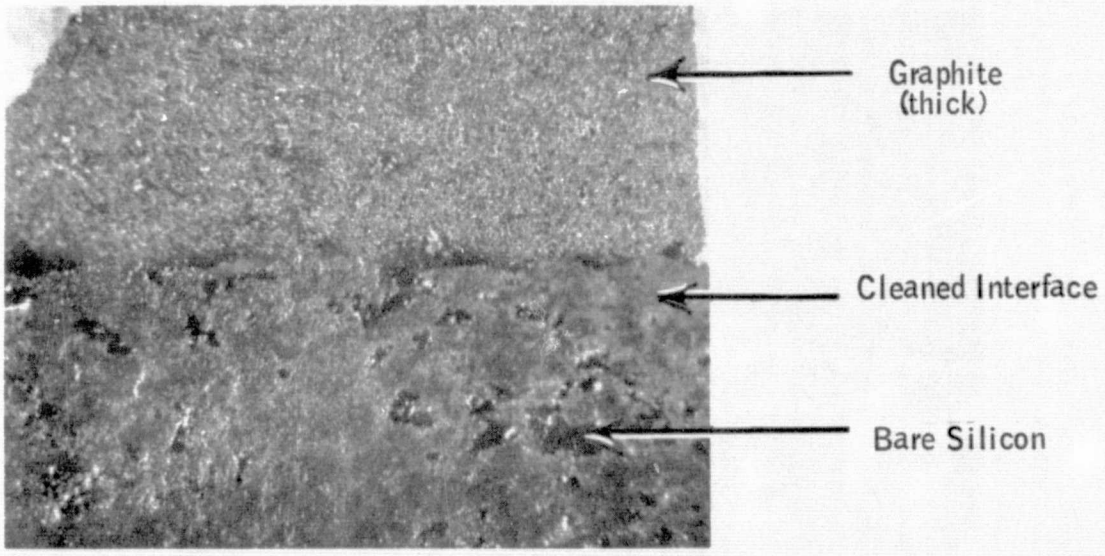


Figure 7. Silicon-Ceramic Interface (unetched) of Substrate MR-8 (200X)



(a) Substrate (30x)



(b) Separated Layer (30x)

Figure 8. Substrate MR-32 and Separated Layer

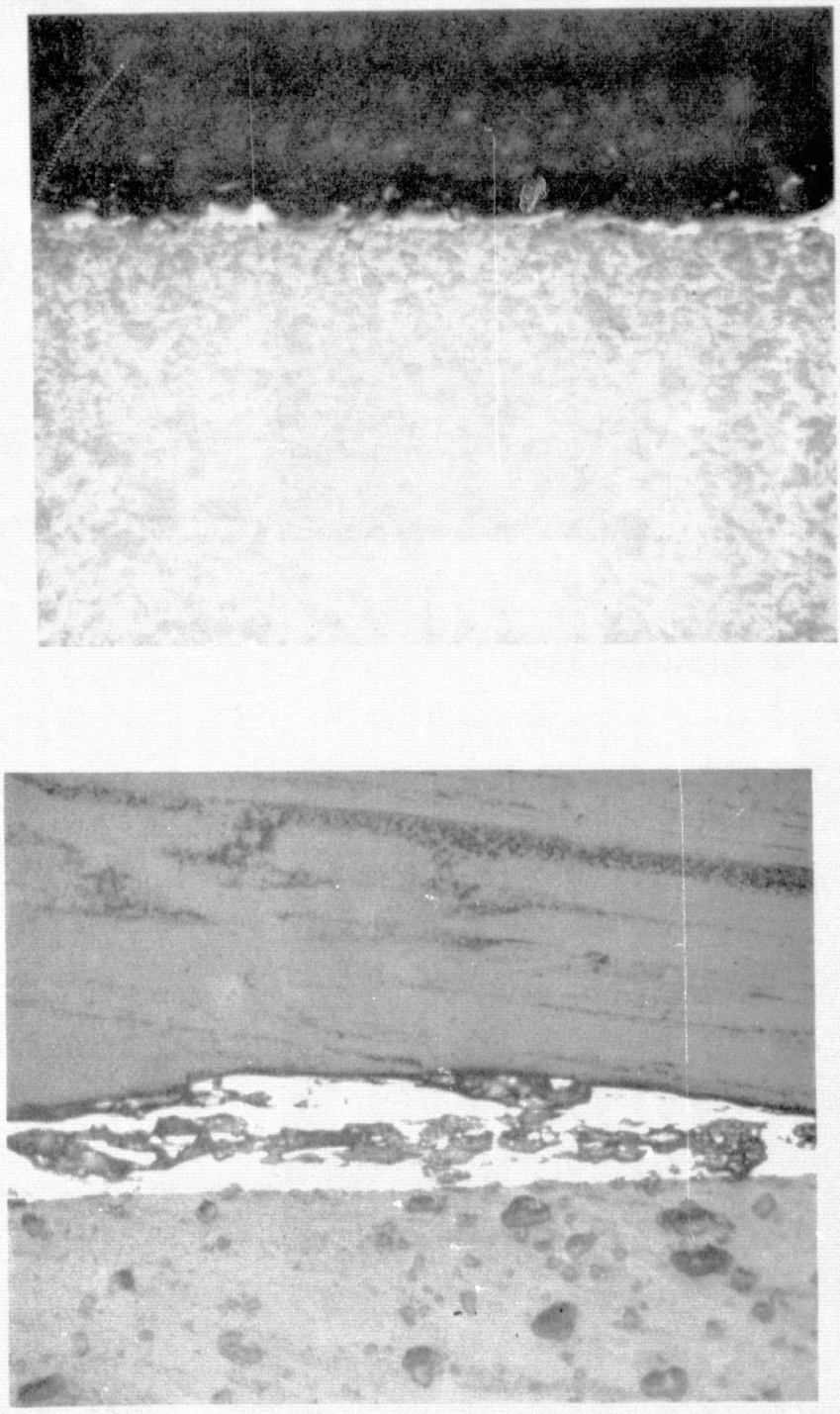


Figure 9. Silicon-Alumina Interface (top) and Silicon-Pressed Mullite Interface (200X)

PHYSICAL PROPERTIES OF SILICON LAYERS

Figure 10 shows schematically the silicon dip-coating growth process as the carbonized ceramic substrate is being withdrawn from the melt; crystallization of the silicon coating occurs along an interface which forms an angle with the substrate as shown. The primary crystallization originates from the solid-liquid interface as opposed to proceeding from the surface of the substrate. Thus, continued nucleation results from previously grown silicon thereby permitting single crystallites, after several millimeters of growth, to enlarge in width as well as in length.

With reference to Fig. 5, all three of these coatings were prepared on rolled, dried and fired mullite substrates. The silicon covered only the side of the substrate that has been coated with carbon. The surfaces of the films appeared bright and shiny to the eye. No cracks were observed in any of the substrates or silicon layers. The top edge of each film had a slightly thicker ridge running across it. Excellent adhesion of the layer to the substrates was noted in the course of handling. The microstructures of all the films were dendritic in nature, with the size of the dendrites dependent on the growth parameters, pulling rate and melt temperature.

Substrate coating MR-1 was pulled at the slowest rate, 0.12 cm/sec, and at a melt temperature of 1434°C. The surface of the sample was covered with gentle ripples running across the film from top to bottom. These were caused by operating the pulling motor controller at too slow a speed, causing jerkiness in the motor. At faster pulling rates, these ripples were eliminated on subsequent coatings.

The dendrites in the microstructure of substrate coating MR-1 were feathery in appearance (see Fig. 11) and typically 1mm wide tending to extend the length of the substrate with the long dimension of the dendrite along the pulling direction. X-ray diffraction showed that the crystallographic surface texture of the film was {1, 0, 0}. The film was 45μm thick.

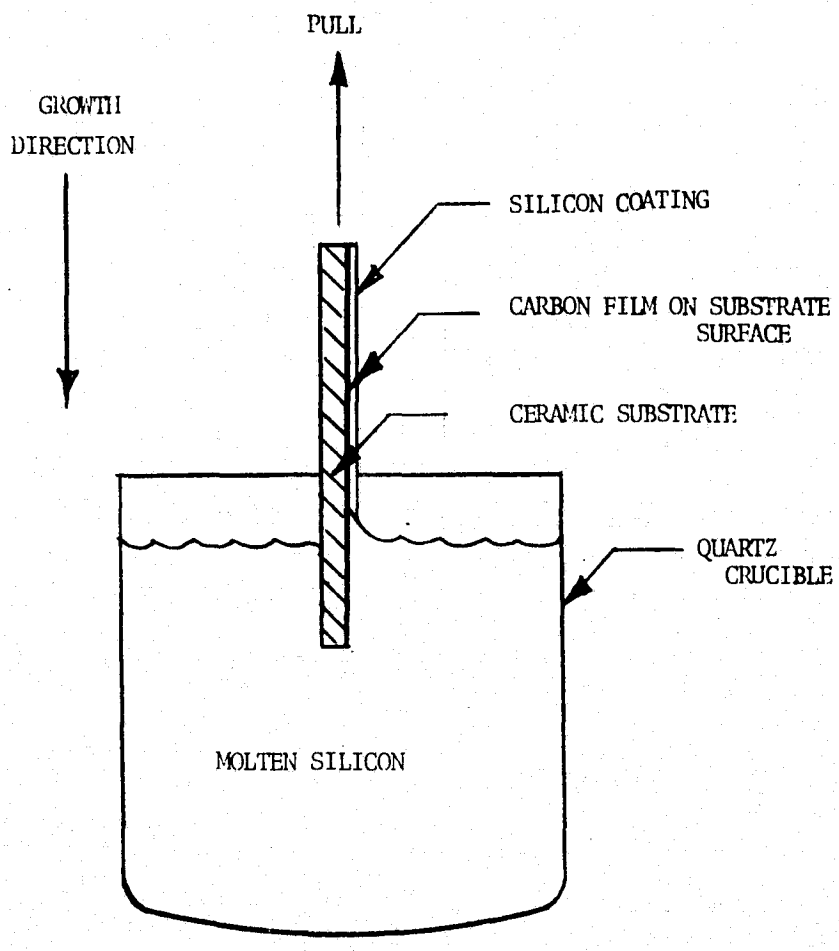


Figure 10. Silicon Dip-Coating Growth Process

Figure 11. Crystalline Grains in Section of Substrate MR-1 (7.5X)

Substrate coating MR-2 was pulled at 0.33 cm/sec from a melt at 1426°C. Its surface appeared quite smooth. The dendrites in its microstructure were more "tree-like" in appearance and were approximately 50μm (2 mils) wide and 250μm (10 mils) long. The long axes were also aligned in the direction of pulling. The film thickness was 12.5μm (0.5 mil).

Substrate coating MR-3 was pulled at 0.33 cm/sec just above the melting point of silicon. The microstructure of this sample was dominated by coarse dendrites emanating from the leading edge of the film. The needle-like main branch of these dendrites were often 1mm wide and 1cm to 2cm long. The surface was not smooth due to the varying thicknesses of these dendrites. Film thickness ranged from 25μm (1 mil) to 150μm (6 mils).

The dendritic nature of the films is indicative that supercooling of the melt existed in all cases before solidification. The various dendritic morphologies reflect the degree of supercooling. Most encouraging is the fact that in all the films there was evidence that the first solidification occurred at the leading edge of the film. This suggests that, under proper conditions, nucleation and growth can be controlled and both grain size and quality improved.

The slightly thicker ridge of material at the top of each film is a consequence of the manner in which pulling was started; i.e., it took a finite amount of time to reach the desired pulling rate, and the film grew thicker at the slower rates.

Figure 12 shows a typical etched cross section of a substrate revealing twin and grain boundaries. Examination of such cross sections showed that the twin and grain boundaries usually run from the substrate to the surface, indicating that the layer consists mainly of a single layer of crystals. In a few instances some overgrowth was noted in small portions of the film, in which case that portion of the film consisted of two or three crystals on top of each other. A similar metallographic analysis was performed by Dr. Martin Leipold of JPL with very similar results and conclusions.

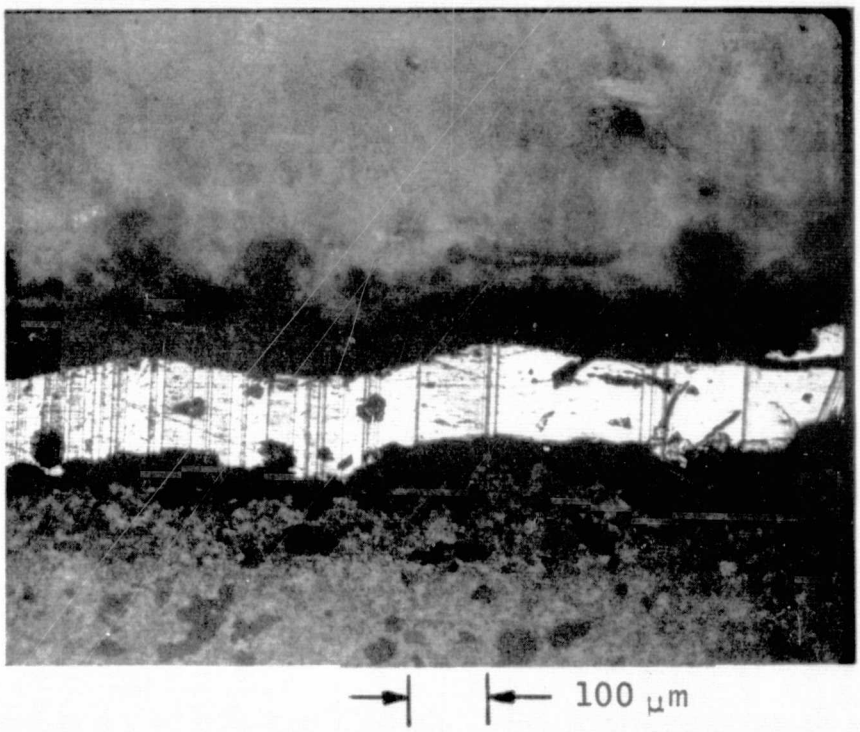


Figure 12. Etched Cross Section of a Typical Dip-Coated Layer (100X)

Since there are relatively few boundaries which run parallel to the surface of the silicon layer, this condition in a solar cell configuration should greatly reduce the number of recombination centers for photon-generated hole-electron pairs generated above or below the space-charge region. Attempts, to date, to ascertain the dislocation density of coated layers by etch and SEM techniques have proven impossible due to the thinness of the layer. Etched holes do occur, but none had the character which could be identified as a dislocation.

Throughout the course of this reporting period, numerous silicon coatings have been routinely grown on inexpensive rolled, dried and fired mullite. The vast majority of these coatings have had excellent adhesion to the substrate and have been free of cracks. The individual crystalline grains have been of the order of 1mm wide and tend to run the full length of the substrate. The major substructure within these grains are twin boundaries.

ELECTRICAL PROPERTIES OF SILICON LAYERS

Since n- or p-type silicon junctions with base-layer resistives of 1 to 3 ohm-cm can produce moderately efficient solar cells, we chose to dope our silicon melt to a concentration level of 5.65×10^{15} boron atoms/cm^{-3} (~2.5 ohm-cm). The integrity of the dip-coating apparatus was checked by melting a boron-doped silicon charge and subsequently checking the conductivity type and resistivity of several of the largest crystalline grains of the solidified charge. Since the resistivity did not change, the system was proven to be free of electrically active impurities at the 10^{15} cm^{-3} level.

As rolled, dried and fired mullite substrates were dipped into this melt, however, the resulting coated layers had p-type conductivities with varying resistivities all of which were less than the intentional doping level of the melt. Had the resistivities been higher than expected, this could have been explained because of the polycrystalline nature of the layers where grain boundary scattering is known to lower the carrier mobility for a given impurity level.

Early in the program, based on relatively few samples, a pattern appeared to develop which indicated that the resistivity of thicker silicon coatings (as measured by the four-point probe method) was generally larger than the resistivity of thinner coatings. Since the four-point resistivity probe measurements were valid only for layers placed on insulators, it was initially postulated that the carbon film between the substrate and the silicon coating was contributing to the overall electrical conduction of the layer. As additional samples were measured, and with the metallographic analysis revealing the discontinuous nature of the silicon-substrate interface, the probability grew that this postulate was in error. Examination of the average resistivity data in Table 1 tends to refute this original resistivity layer thickness trend. The free carbon which appears to exist in islands at the silicon-substrate interface may, in some complex way, affect the conductivity of the coating. This effect, however, cannot be understood until we know more about the carbon-silicon interface. The islands of carbon could, in fact, play some part in the nonuniform resistivity observed over the surface of large-area coatings.

Since the primary means for determining the doping levels of these dip-coated layers has been with the four-point resistivity probe, consideration was given to evaluating these layers using Hall measurements. The four-point probe technique gives an accurate measure of resistivity if the thickness of the layer is known, but the carrier concentration is obtained by assuming that the mobility in the polycrystalline layers is the same as in single-crystal silicon. This assumption, in general, is not valid; therefore, three Hall samples were prepared from two dip-coated substrates (MR-1 and MR-7). In addition to these three samples, an additional Hall sample was prepared from a silicon melt (run 8) which had only mullite substrates dipped into it. This particular melt did, however, have the final mullite substrate solidify in it and remain in the melt during the facility shutdown procedure. Of the three samples prepared from dip-coated layers, two were prepared from substrate MR-7 which also had the melt surface solidify around it. This required it to soak in the melt for 9 minutes before remelting was accomplished and

temperature equilibrium could be established. In a sense, the samples prepared from MR-7 thus represent a worst-case example as far as time allowed for the substrate to contaminate the silicon coating. The remaining substrate was prepared from MR-1 which represents a more typical time in which the substrate is in contact with the molten silicon.

Preliminary measurements have been made on these three dipped layers and on one bulk polycrystalline sample taken from melt 8 to determine, first, if the resistivity measurements can be used to determine the carrier concentration and, second, how the carrier concentration in the layers compares with the starting concentration in the melt.

These Hall samples were prepared from the layers by masking the sample configuration and sandblasting the remaining silicon from the substrate. The samples were about 1cm long and 1mm to 2mm wide, with the voltage side arms about 5mm apart. Contacts were made by evaporating Al and alloying at 750°C for 10 minutes. Electroless Ni was plated over the alloyed Al and In soldered to the Ni. The bulk polycrystalline sample was made in essentially the same manner except the thickness was 0.063cm rather than the 40μm to 50μm typical of the layers. The measurements were made in a standard manner using a d-c field of 2K gauss.

A summary of the room temperature measurements is given in Table 5. The sample designations MR-7-P and MR-7-X refer to the crystalline orientation in the Hall sample, with "P" meaning the long axis of the grains were parallel to the direction of current, and "X" meaning the long axis of the grains were oriented across the sample, perpendicular to the direction of current. As seen in Table 5, these two samples have slightly different mobilities, with the highest mobility in sample MR-7-P. The mobilities in all four samples is lower than the 250 to 300 cm^2/volt sec expected for single-crystal material with carrier concentrations in the 0.6 to 2 x 10^{17}/cm^3 range.

Table 5. Summary of 300°K Electrical Properties

Sample No.	Carrier Conc. (cm^{-3})	Resistivity (ohm-cm)	Mobility (cm^2/V sec)
MR-7-P	6.7×10^{16}	0.45	208
MR-7-X	7×10^{16}	0.6	146
MR-1	7.5×10^{16}	0.54	153
Bulk Poly (Melt-8)	1.8×10^{17}	0.24	146

The temperature dependencies of carrier concentration, resistivity and mobility for sample MR-7-X are shown in Fig. 13 and 14. In general they behave as expected for silicon; the carrier concentration decreases and the resistivity goes through a minimum before increasing as the sample is cooled. The one exception occurs at 77°K where the carrier concentration apparently increases over the 85°K value. The temperature dependence of the mobility is compared with a single-crystal sample with a carrier concentration of $2 \times 10^{17}/cm^3$ in Fig. 14. The notable difference is the sudden drop in mobility in the layers at 77°K. No explanation for this decrease is postulated at this time.

An attempt was made to measure the electrical properties of the bulk polycrystalline sample below room temperature, but the results were not sensible and will not be reported here. Since this bulk sample was prepared from a solidified melt it could likely have had small cracks or voids in it which could explain the anomolies experienced below room temperatures.

The main point to note from these measurements is that the mobility in polycrystalline samples will be lower than in a single-crystal sample with the same doping density. As a result, the resistivity measurements will indicate a higher purity by as much as a factor of two.

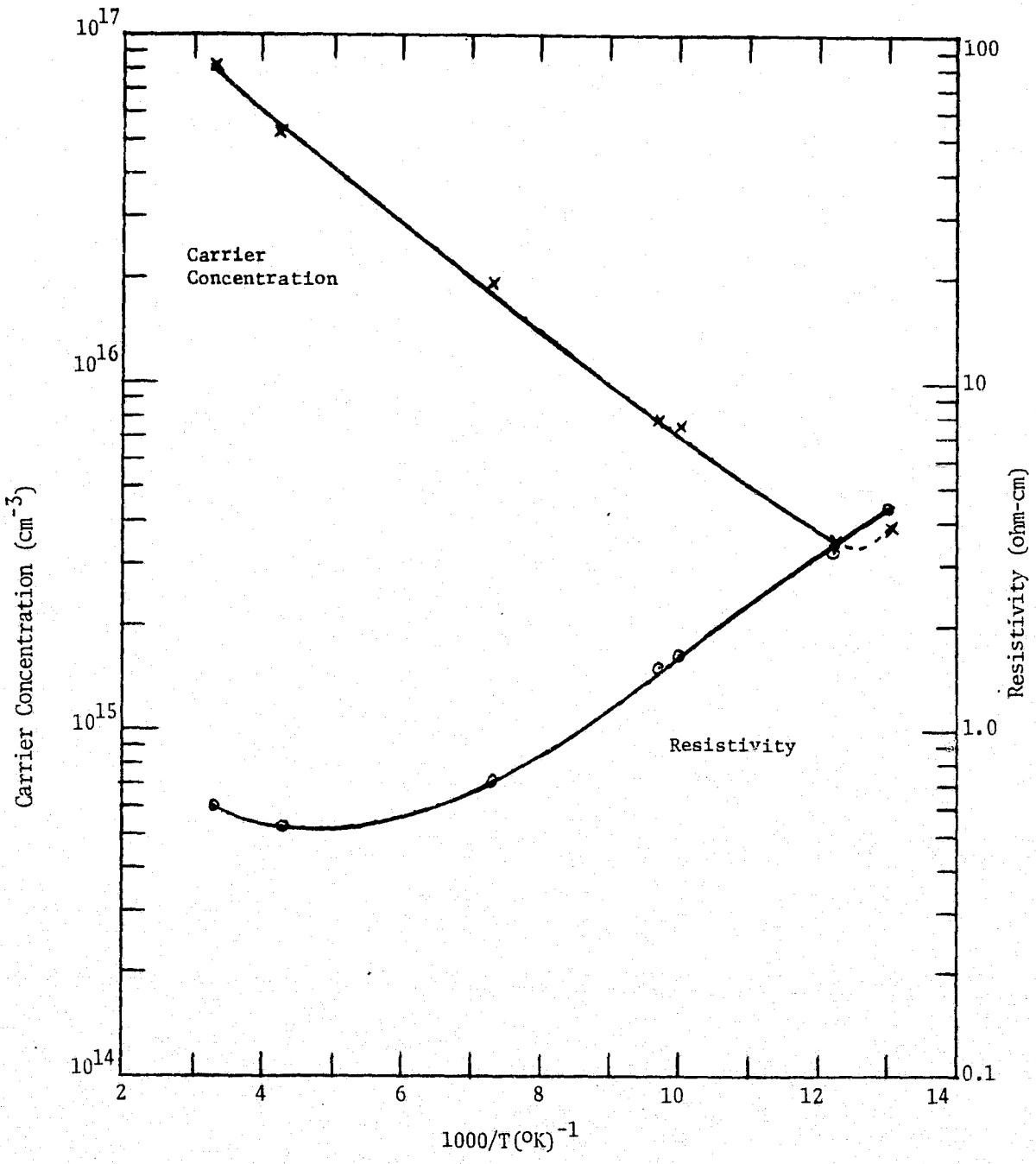


Figure 13. Carrier Concentration and Resistivity versus 1000 (°K)$^{-1}$

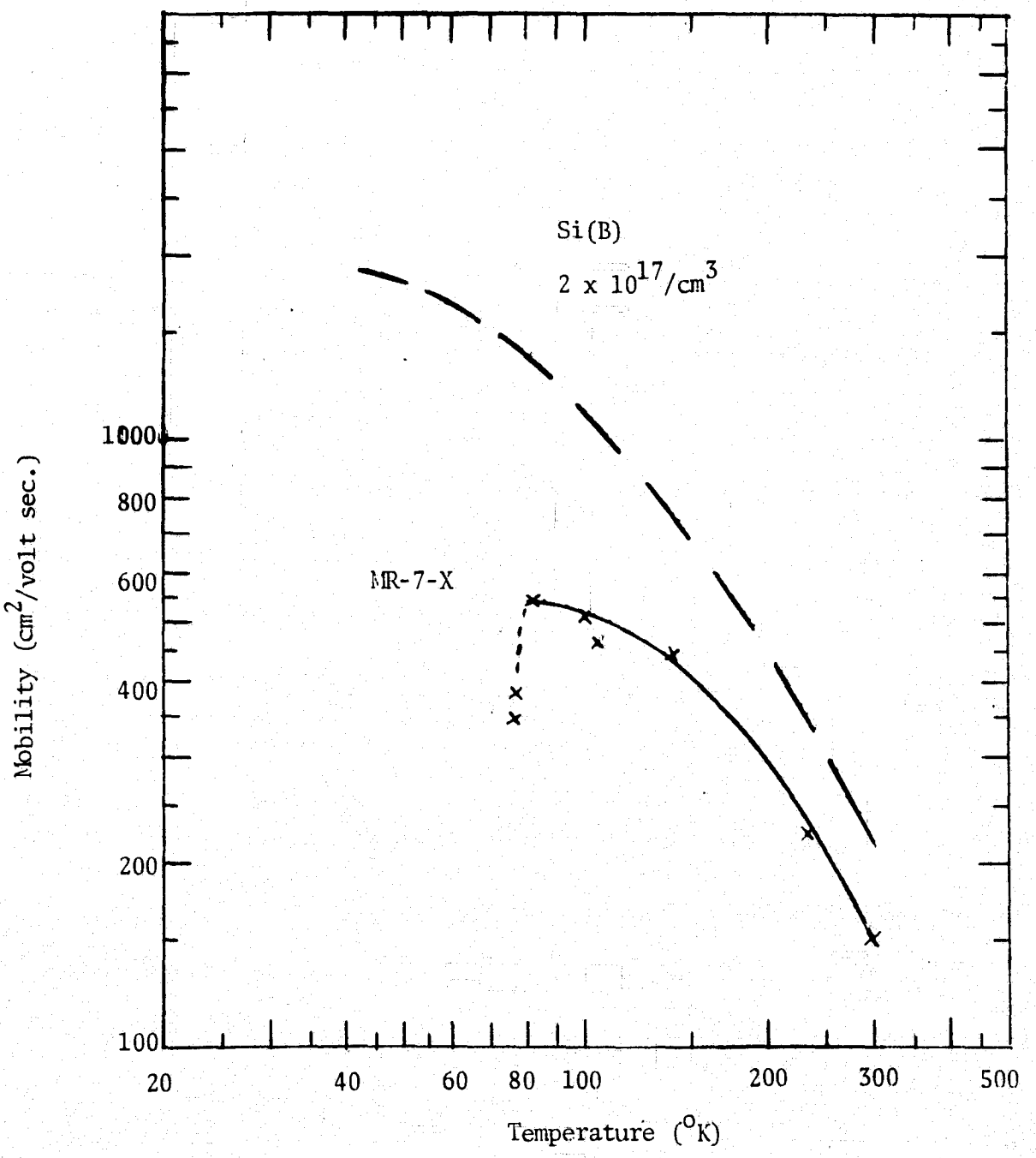


Figure 14. Mobility versus Temperature (°K) for Sample MR-7-X and a Single Crystal

The second point is the doping level in the melt after solidification. The crucibles are loaded to produce 2.5-ohm-cm ($5.65 \times 10^{15}/cm^3$) p-type crystals. The one bulk sample measured indicates a lower resistivity after layers have been dipped. There is some question as to the reliability of these measurements, but the doping level is apparently higher than expected. Further measurements will have to be made on other melts to determine if this occurs regularly.

To investigate the source of this excess p-type conductivity in melt 8, a thin wafer was prepared from this melt, and a 10°K infrared transmission measurement was made using an FTS-14 Fourier Transform Spectrometer. The absorption coefficient is shown in Fig. 15 as a function of photon energy in cm^{-1} [$\lambda(\mu m) = 1 \times 10^4/°K(cm^{-1})$]. The prominent absorption lines are labeled according to the standard nomenclature for acceptors in silicon. At the lower energies, three lines due to boron are clearly seen and are labelled 1 through 3. At the higher energies a number of lines characteristic of aluminum (Al) are seen, labelled X1, X3, 1, 2 and 4. The most prominent Al line (line 2) is totally absorbing in this particular sample because of the relatively thick sample used at this high carrier concentration.

An estimate of the impurity concentrations of both boron and aluminum can be made from the intensity of the absorption peaks. These are $(4 \pm 1) \times 10^{15}/cm^3$ for the boron and $(8 \pm 4) \times 10^{16}/cm^3$ for the aluminum. The Al concentration is more uncertain than our estimate of the boron concentration since we have not run a standard with Al doping. We have had to rely on Al spectra which have appeared in the literature. The boron concentration in the sample is approximately the amount loaded in the melt, but less than the aluminum.

The first and most obvious conclusion to be made from the above measurement is that mullite is being dissolved by the molten silicon. This is probably true, but it would be a mistake not to consider the possibility of some coincidental source caused by uncleanness in the substrate processing technique or

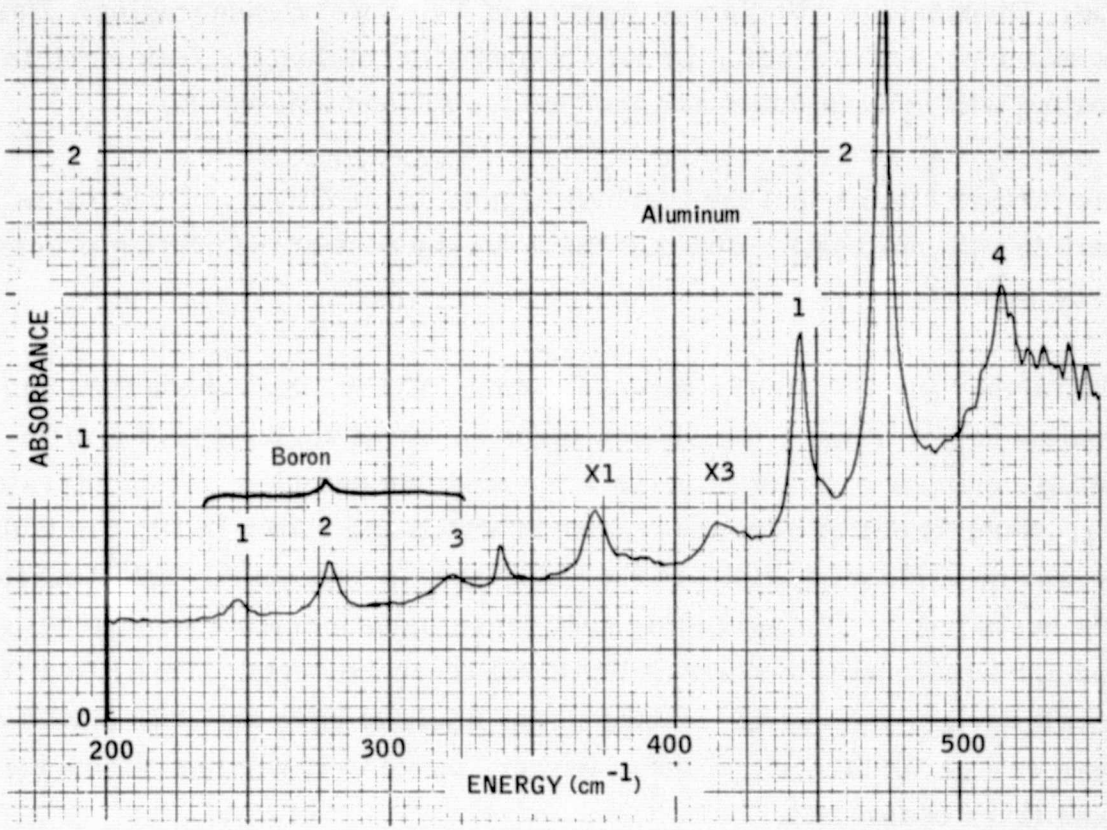


Figure 15. Absorbance Spectrum of a Polycrystalline Silicon Sample from Melt 8 (The boron lines are indicated and labeled as 1-3; the remaining absorption lines are due to aluminum)

the impurities in the carbon coating. Tylan Corporation of Torrence, Calif., has been requisitioned to coat all surfaces of four MV-20 rolled, dried and fired mullite substrates with their reportedly impervious glassy carbon coating. Discussions with James Warren of Tylan were encouraging. Based on his experience with coating impure graphite crucibles, he feels certain that his coating will remain intact and that molten silicon will wet it.

He further claims that the thermal expansion coefficient of mullite is compatible with his coating and that the scale-up cost of the coating process would be modest.

To further investigate the extent to which, if any, the carbon film has on the overall conductivity of the silicon layer, several angle-lapped profile-spreading resistance measurements were made on samples from substrate MR-12. Several scans were made, two of which are shown in Fig. 16 and 17. There was no evidence that the carbon coating was appreciably affecting the layer's resistivity. The spreading resistance measurements were generally in good agreement with the four-point probe measurements. Thus, in a final solar cell device, the carbon coating is not likely to have any deleterious effect on solar cell performance and may, in fact, serve to lower the resistance of the base layer of the cell.

The angle-lapped profile measurements further support the belief that little or no SiC is formed from the carbon coating on the substrate when it is immersed in molten silicon. The dark regions on the photographs in Fig. 16 and 17 were originally believed to be SiC and/or free carbon. Note that, as the spreading resistance probe touches the dark region in Fig. 16, there is a sudden drop in resistance, whereas, when the probe touches the dark regions in Fig. 17, there is a sudden increase in resistance. One possible explanation for this inconsistency is that perhaps little or no carbon is converted to SiC and that, upon angle lapping the sample, this free carbon may or may not be lapped away. The absence of carbon could show up as a dark region on the photograph because of the coaxial illumination.

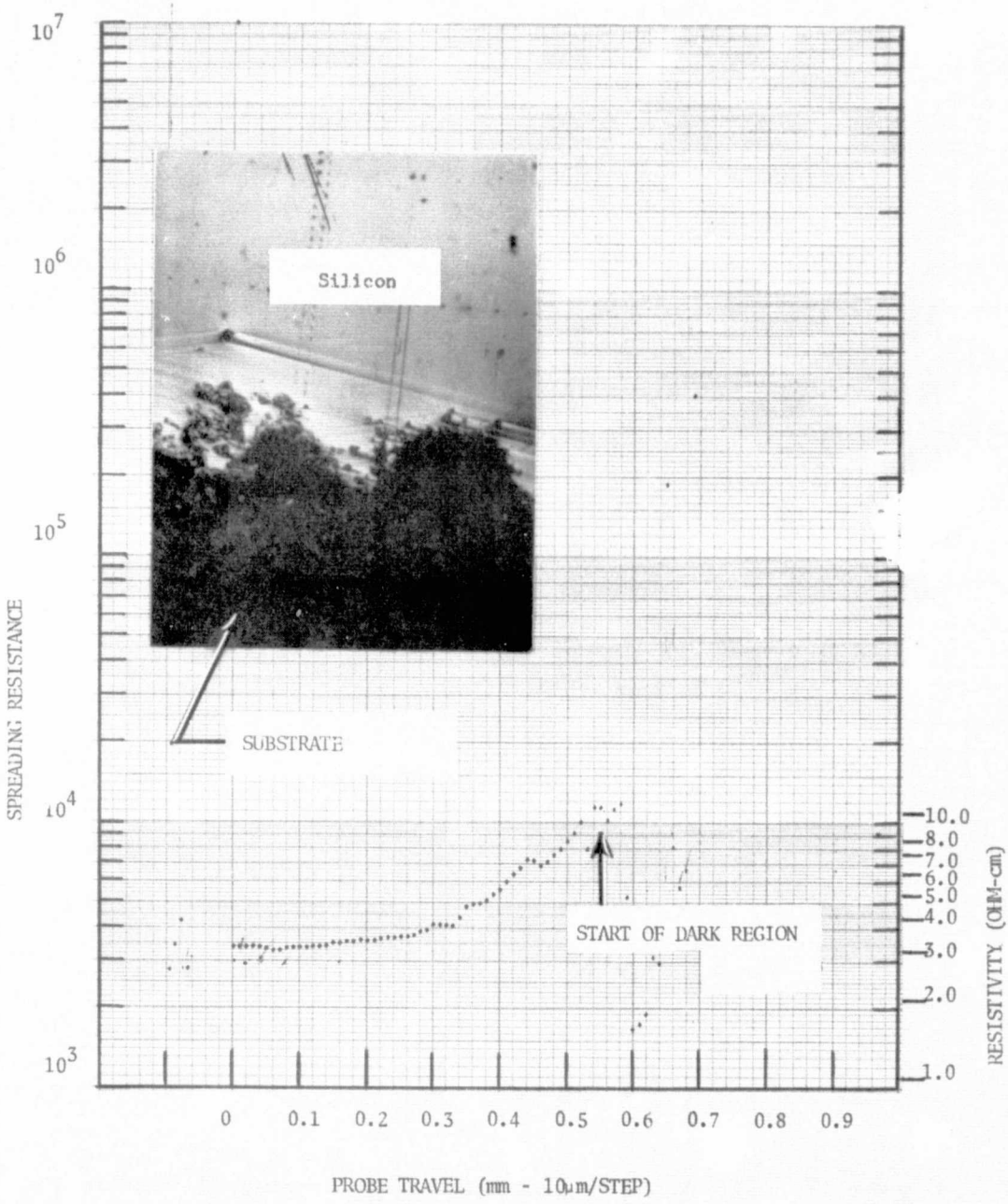


Figure 16. Spreading Resistance – Angle-Lapped Profile on Sample MR-12-4, Scan A-1

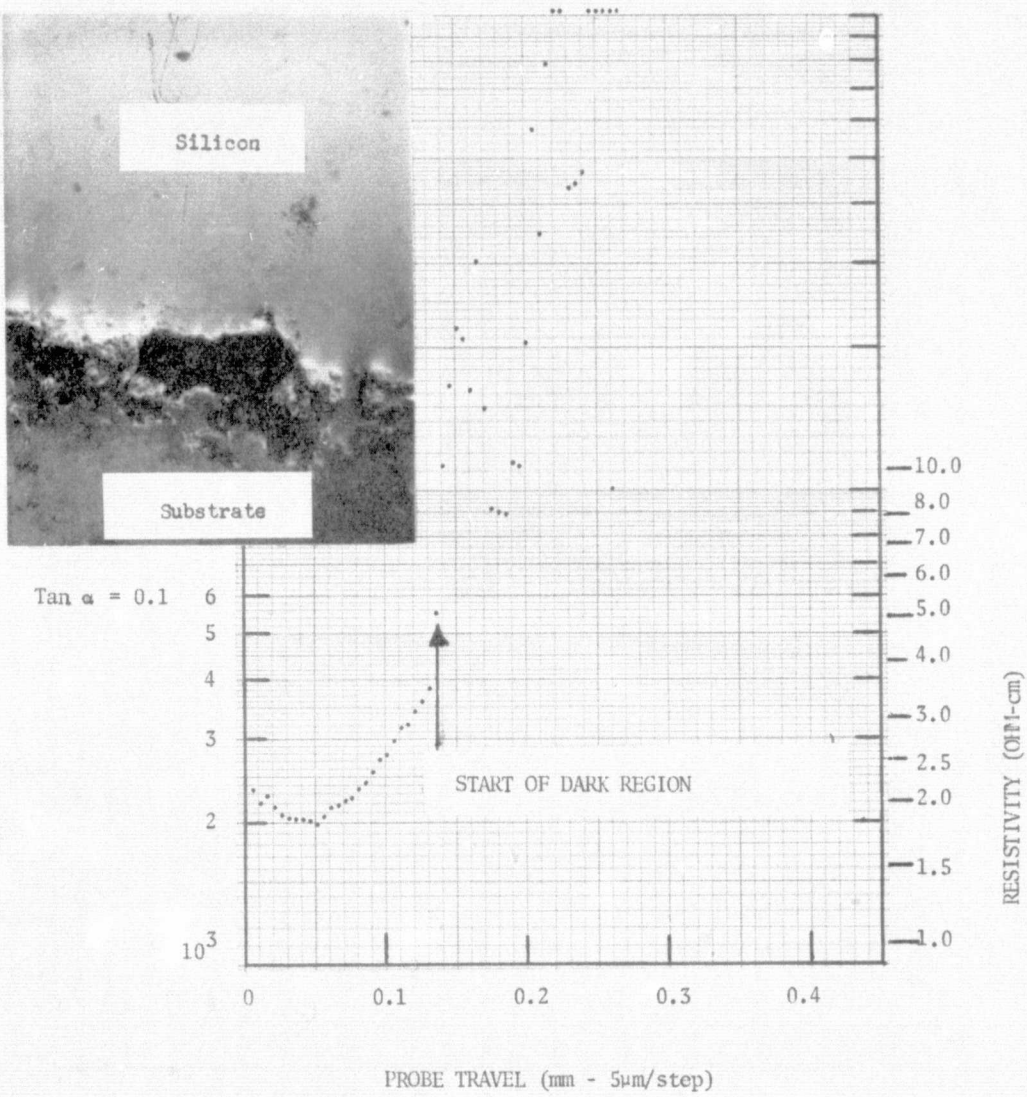


Figure 17. Spreading Resistance – Angle-Lapped Profile on Sample MR-12-4, Scan SS-2

Figure 18 is a spreading-resistance surface scan on a sample from MR-12. Over the small distance scanned (0.45mm) the resistivity was reasonably uniform and only slightly larger than that measured by the four-point probe. It is encouraging to note that, as the probe crossed twin boundaries in steps of 5μm, little or no change in resistance occurred. On the other hand, there was about a factor of two increase in resistance at the single-grain boundary in Fig. 18.

CHEMICAL PROPERTIES OF SILICON LAYERS

Since the starting silicon of the dip-coating process is high-purity semiconductor-grade silicon stock, any contaminating chemicals contained in the finished layers must originate from one or more aspects of the dip-coating process. The most likely contaminating source, and one presently under suspicion, is the ceramic substrate itself. Within the resolution limits of EDAX (see Fig. 19) and a Scanning Auger Microscope analysis no contaminating elements have been observed. The discovery of aluminum by the IR transmission measurements, discussed in the previous subsection, suggests that the rolled, dried and fired mullite substrates may, to some degree, be dissolving in the molten silicon. Should this be the case several chemical impurities within this particular grade of mullite would have to be considered. Table 6 lists the chemical composition of the McDanel MV-20 mullite composition from which these substrates are made. Since the process by which these substrates are made or the carbon coating on the substrate itself, could also be a contamination source, both must be cleared before one can say with certainty that mullite is dissolving. To date this is an area of study that has not been undertaken.

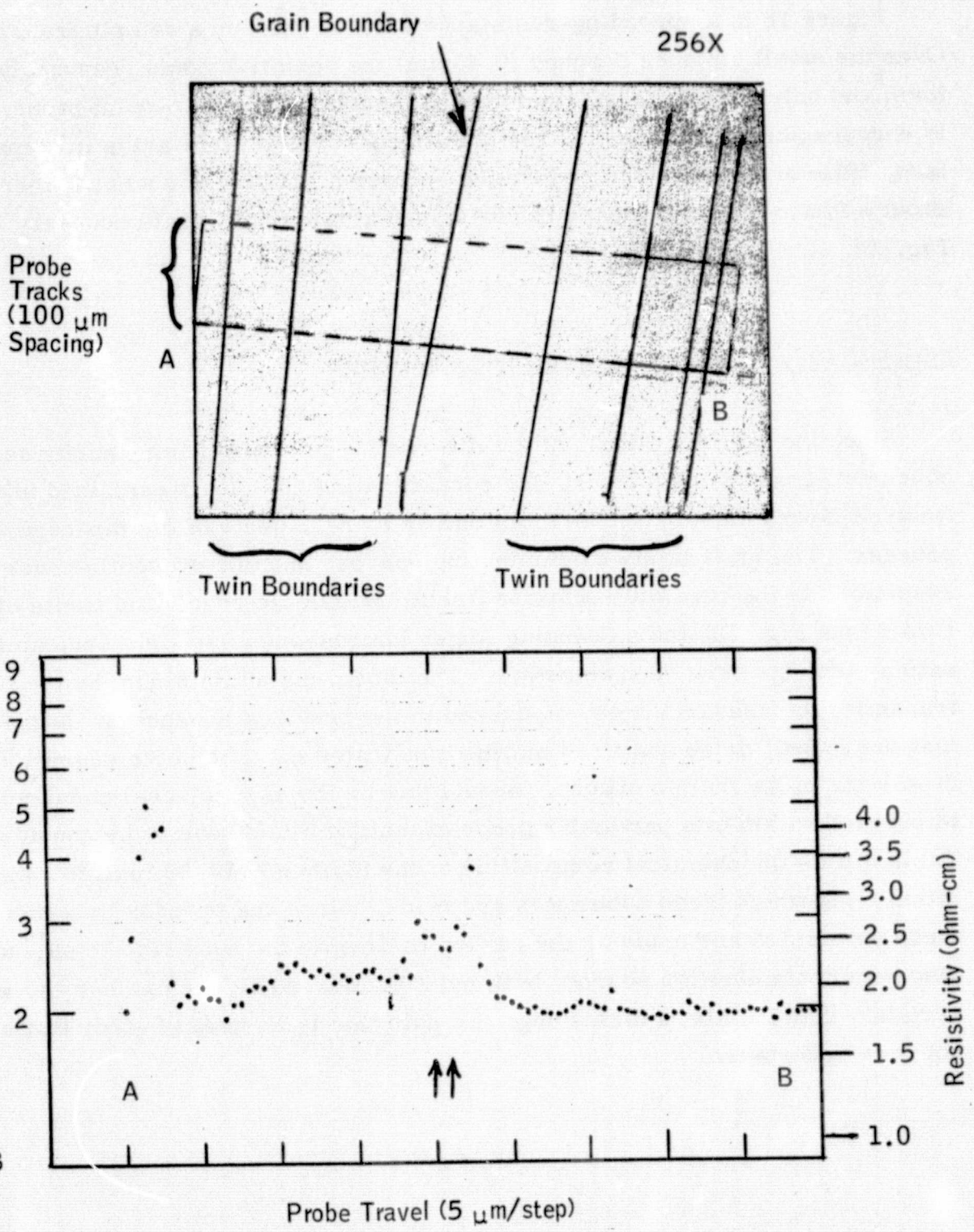
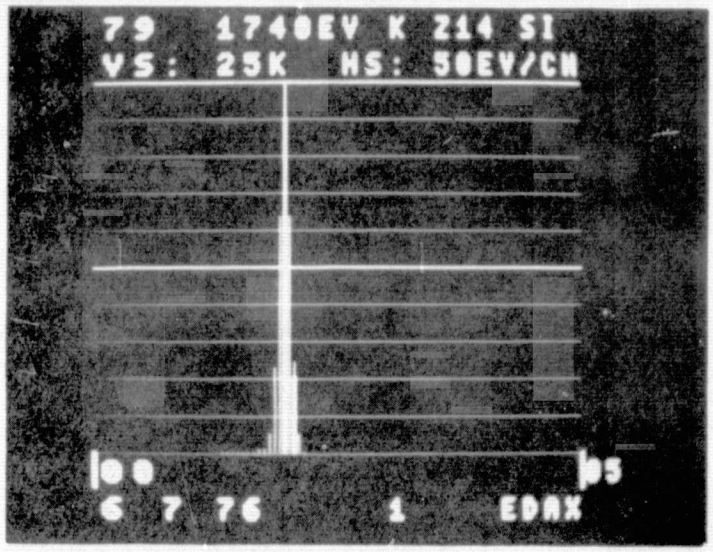
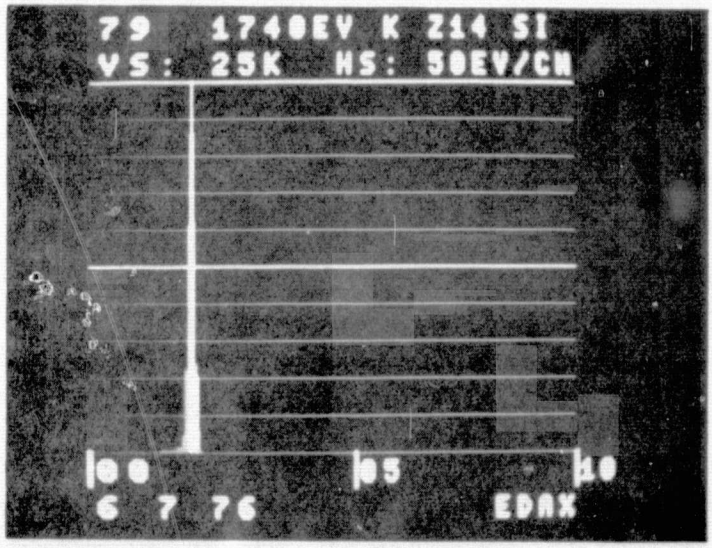


Figure 18. Spreading Resistance - Surface Scan on Sample MR-12-4



(a) MR-1



(b) MR-7

Figure 19. EDAX Analysis of Samples from Substrates MR-1 and MR-7

Table 6. Chemical Composition of McDanel MV-20 Mullite

Material	Percentage	Melting Point
Al_2O_3	55.4	2045°C
SiO_2	42.0	Nat. quartz 1610°C, crystalline 1713°C
MgO	0.4	2800°C
Na_2O	0.5	Sublimes at 1275°C
CaO	0.1	2580°C
Fe_2O_3	0.8	1565°C
TiO_2	0.5	1830° to 1850°C
K_2O	0.7	Decomposes at 350°C

DIODE PROPERTIES

Diode Fabrication

To fabricate and evaluate the photovoltaic properties of the dip-coated layers, junction diffusion and electroding techniques must be developed. Thus, a p-n junction diffusion furnace was assembled (see Fig. 20), and time was spent investigating various electroding techniques. Single-crystal solar cells were fabricated in an effort to reacquaint ourselves with the art of achieving proper junction depths (X_j) with large top-surface concentrations (C_s). We have not yet fully optimized all parameters which contribute to high conversion efficiencies but are presently able to routinely fabricate 8% to 9% efficient single-crystal solar cells with a C_s greater than 10^{20} cm^{-3} and fill factors (FF) on the order of 0.7. The above reported efficiencies are without the benefit of classical AR coatings or optimized top-layer electroding techniques. Producing electrical contacts with good adhesion in either the single-crystal wafers or the dip-coated layers remains a problem. Our best

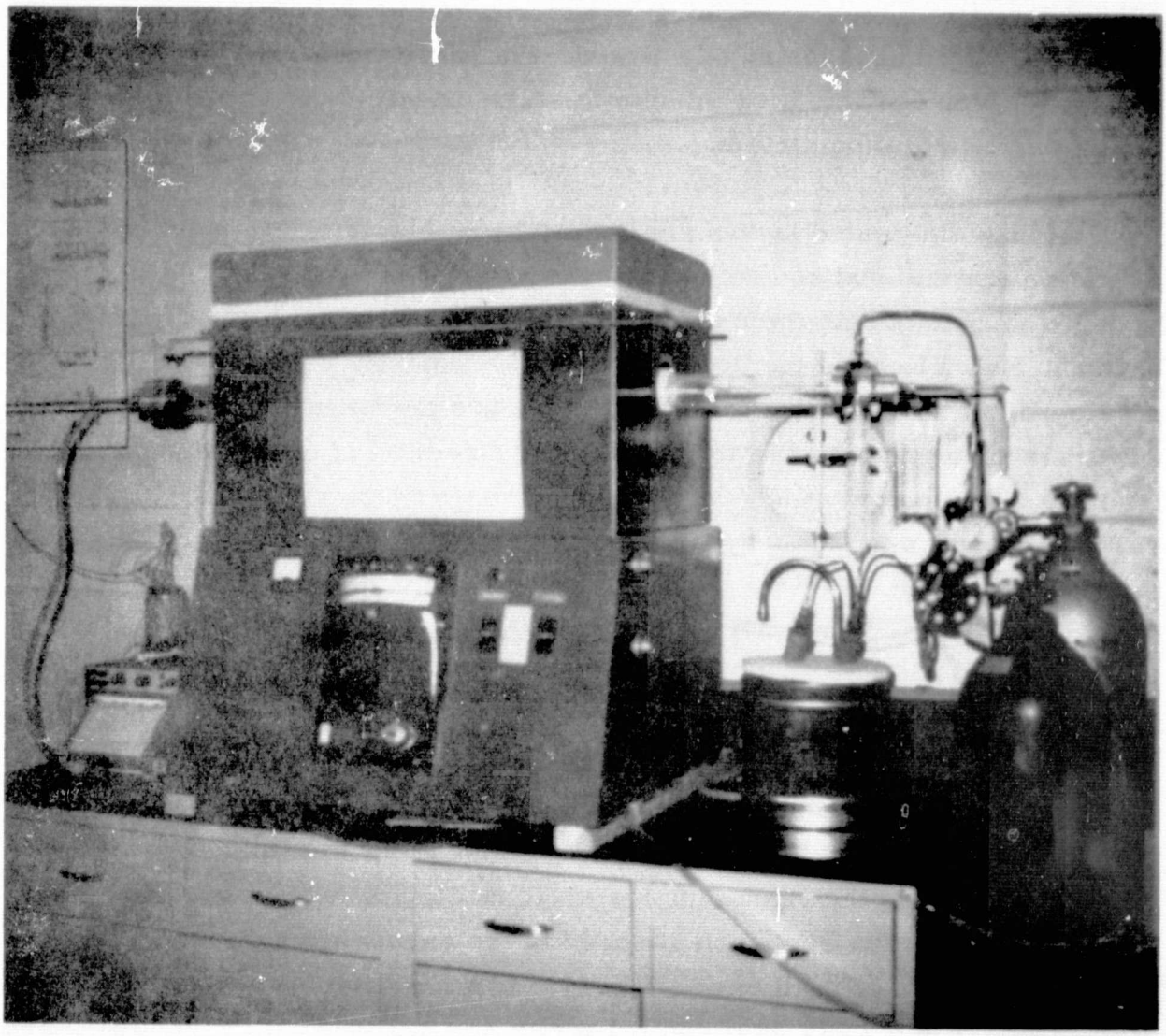


Figure 20. Diffusion Furnace

electrodes have been electroless nickel. The more traditional evaporated titanium-silver contacts give inferior results, possibly due to the poor condition of our evaporation station.

Because dip-coated layers are backed by an electrically insulating ceramic, conventional contact to the base layer is not possible. Initially we intended to contact both the p and n region of the cell via the top surface as shown in Fig. 21, but a method believed to be superior has since been developed. If narrow (50μm to 100μm) slits are preformed in the ceramic substrate such that they are in line with the direction of crystalline growth (see Fig. 22), molten silicon will "wick" through these slits to the back side of the substrate when it is dip-coated. The back surface of the substrate can then be metallized. For the purpose of our present investigation, however, contact to the base layer will not be made in this manner.

"Mesa-type" diodes have been fabricated by the method shown in Fig. 23. Note that contact to the p-type base layer was accomplished by angle lapping (2 degrees) one edge of the layer and subsequently applying an electroless nickel plating to this region. Small dots of black wax were placed on the top diffused layer, and the remaining material was lightly etched to form small mesas. Small wires were then attached to the mesas using silver paint. Silver paint was also used to attach a wire to the electroless-nickel-plated base layer. A single-crystal control wafer was diffused with each dip-coated sample and contact to its p-type base layer, and the mesa diodes were fabricated in an identical manner.

Photodiodes have been made on sections from both substrates MR-12 and MR-13, with those on MR-12 having more encouraging results.

Substrate MR-12 was a smooth-surface layer, and, as such, the diffusion took place on a virgin, as-grown surface. It is important to point out that MR-12 had a layer thickness of only 25μm to 30μm and individual crystalline

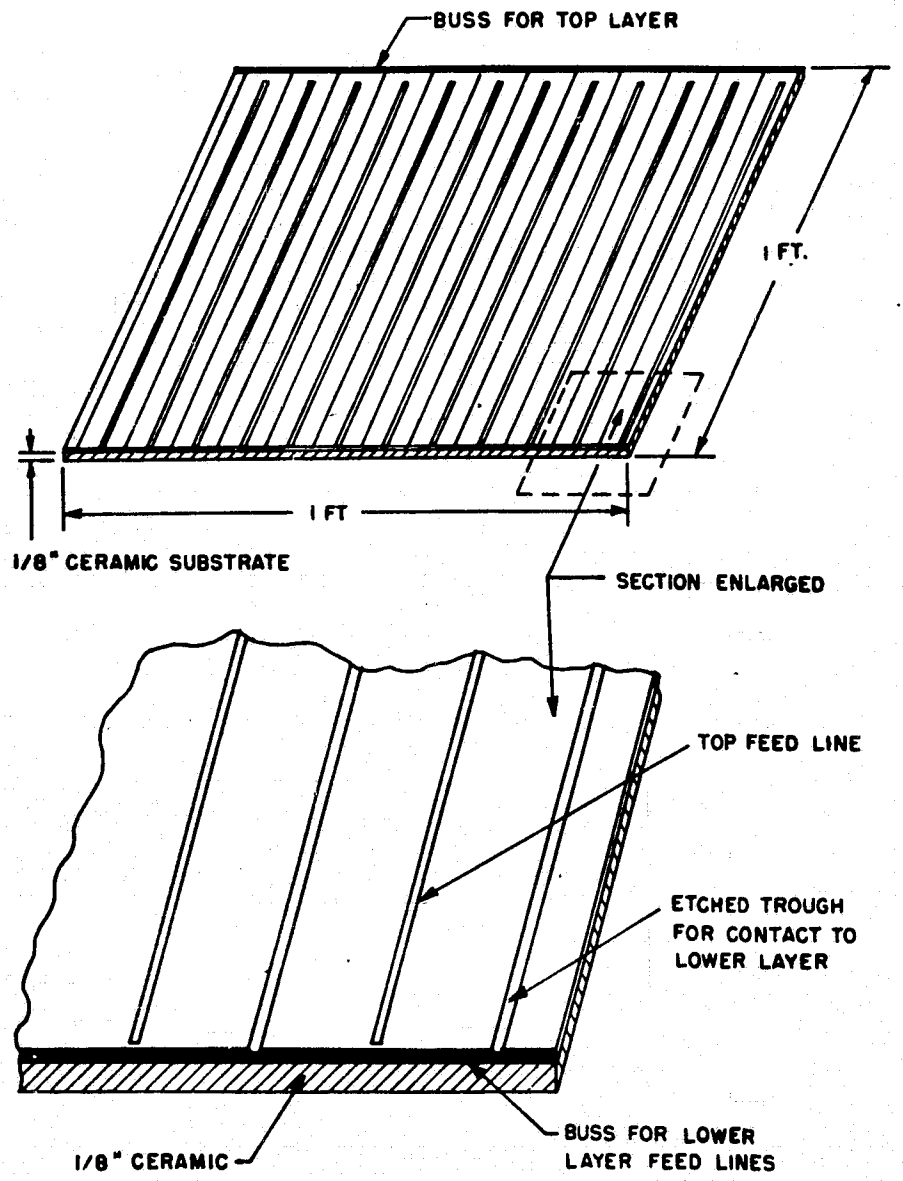


Figure 21. Initially Proposed Solar Cell Electroding Method

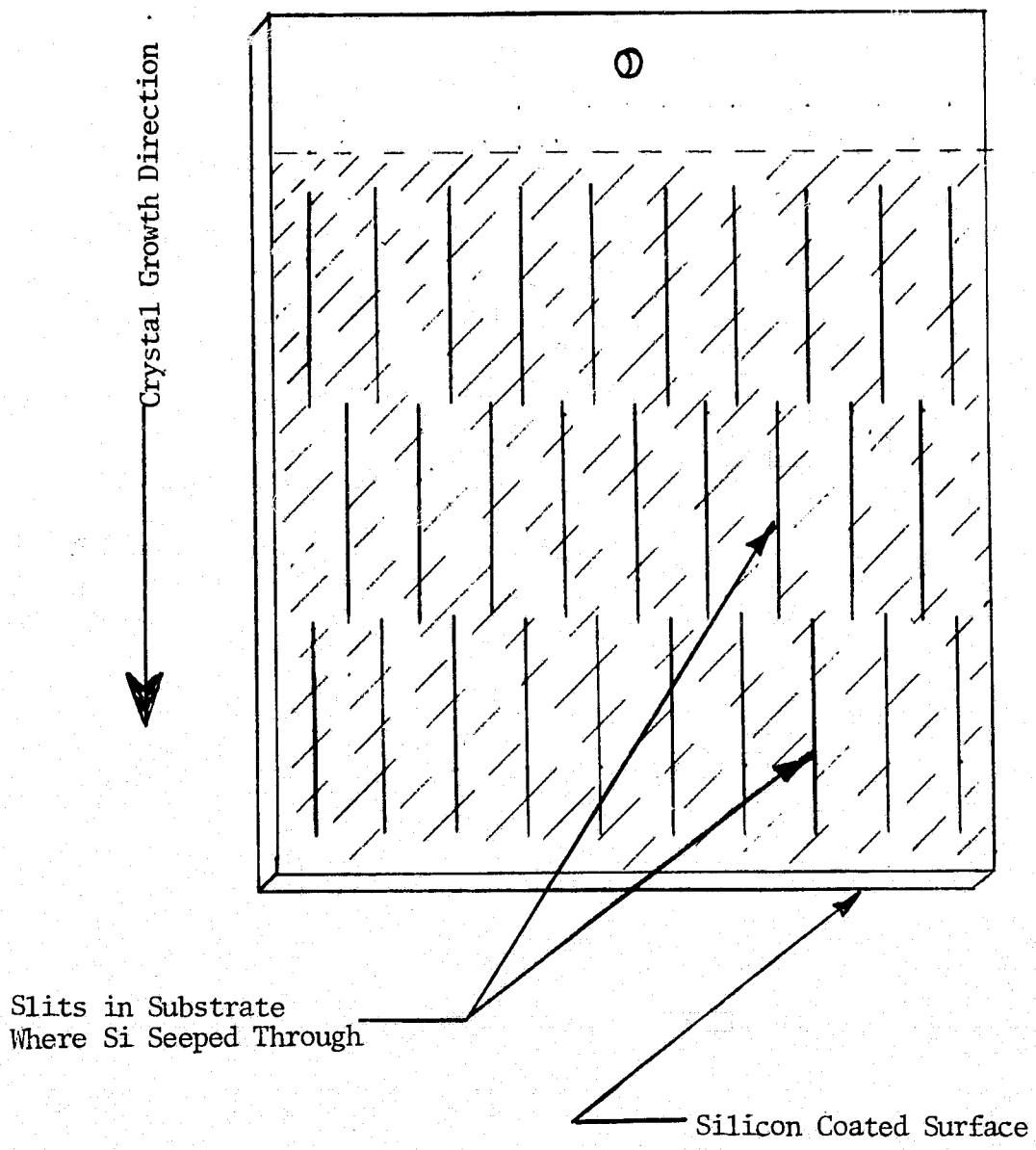


Figure 22. Proposed Base Layer Electroding Method

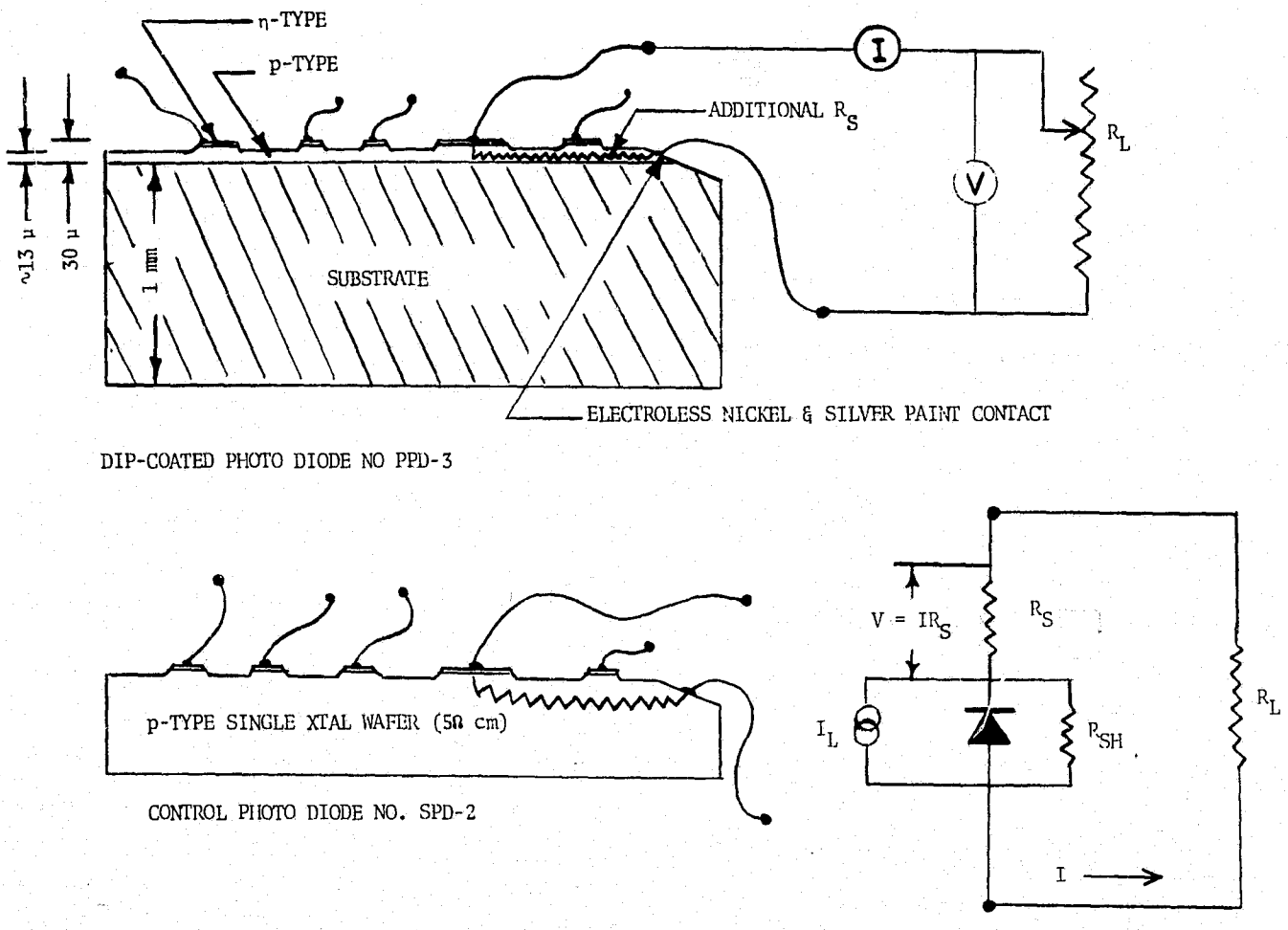


Figure 23. Photodiode Fabrication Method

dendrites somewhat smaller than the 1mm x 1cm to 2cm crystallites previously reported in other layers. No attempt was made to confine the mesas to individual single-crystal grains; thus, several grain boundaries exist in each mesa tested. The largest mesa ($\sim$0.03cm^3 in area) proved to be the most interesting to evaluate. This was principally because its larger area provided enough photocurrent to evaluate its solar cell potentialities. This diode has been designated PPD-3. All the diodes on both MR-12 samples have very similar open circuit voltages.

Figure 23 illustrates the fact that, in the process of forming the mesas on thin layers such as MR-12, only about 12μm to 13μm of base-layer silicon remains between the mesas and the base-layer electrode. This introduces a substantial resistive path in the base layer.

Diode Characteristics

Measurements were made on diode PPD-3 of the photoresponse, the dark I-V characteristics, and the capacitance as a function of voltage. We also measured the diode reverse recovery characteristics in an attempt to determine minority carrier lifetime, but the high series resistance of the diodes gave a simple exponential decay unrelated to lifetime. Measurements of the C-V characteristics were made at 1, 10 and 100 kHz. Figure 24 shows $1/c^2$ as a function of voltage at 1 and 100 kHz. The slope of this line is described by

$$\frac{d}{dV}\left(\frac{1}{C^2}\right) = \frac{1}{q\epsilon A^2}\left(\frac{1}{N_D} + \frac{1}{N_A}\right)$$

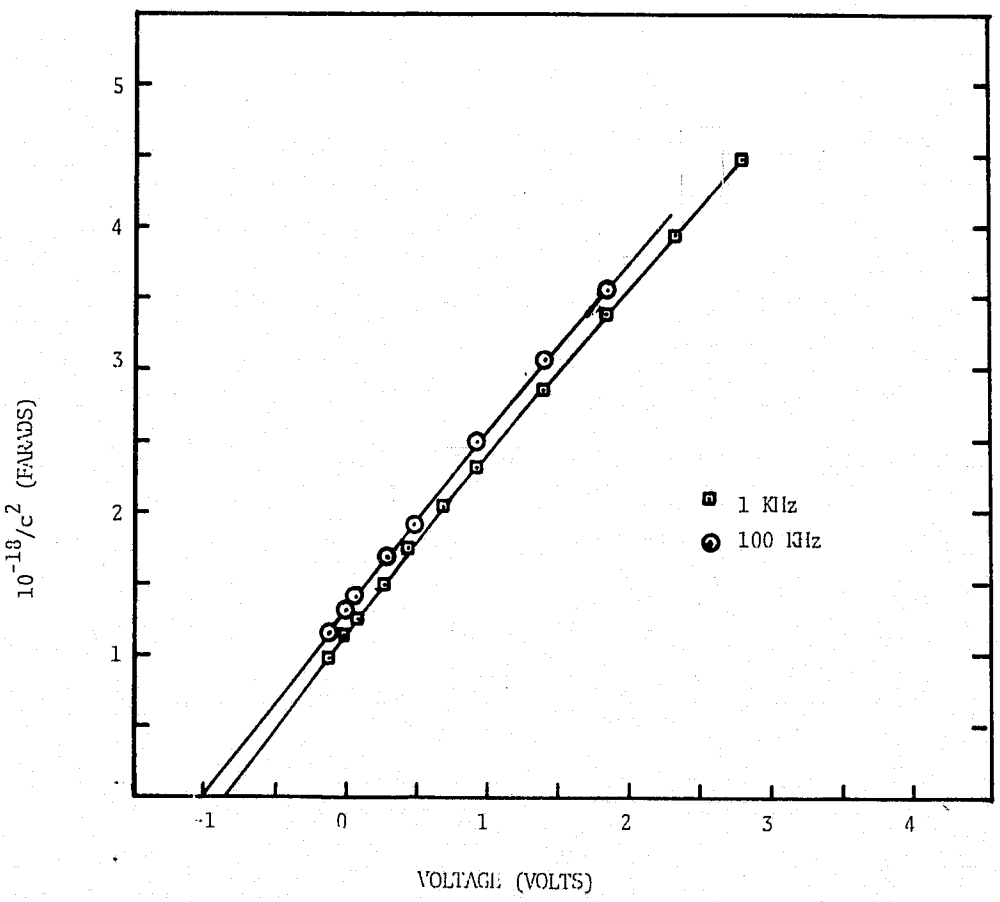


Figure 24. Capacitance-Voltage Characteristics of Diode PPD-3

where

q = electron charge

$\epsilon = \varkappa\epsilon_0$ = dielectric constant

A = junction area

N_D, N_A = donar and acceptor concentrations at the edges of the space-charge regions

Since $N_D >> N_A$, the slope gives the acceptor concentration. Beyond about half a volt of reverse bias, the slope in Fig. 24 is constant and gives an acceptor concentration of 1.12×10^{16} cm^{-3}. The four-point probe measurements on MR-12 gave a resistivity of 1.7 ohm-cm from which a hole mobility of 330 cm^2/volt sec can be derived. This is in the range expected for our polycrystalline layers.

The intercept in Fig. 24 gives a value for the built-in voltage of the junction. In principle, the low-frequency capacitance data should be used, and it extrapolates to a built-in voltage of 0.85, compared to a value of 0.93 which is observed in single-crystal n on 1-ohm-cm p solar cells.[1]

The dark I-V characteristics of diode PPD-3 are shown in Fig. 25. The data are seen to be fit fairly well by an equation of the form

$$I = I_0 (e^{qV/nkT} - 1)$$

where $I_0 = 1.25 \times 10^{-8}$ A and $q/nkT = 21.9$ V^{-1} corresponding to $n = 1.78$. Although the above equation does not fit the reverse current, it does give the right order of magnitude.

It is of interest to compare the measured I-V characteristics with theoretical expressions[2, 3] for the I-V characteristics. It is well known

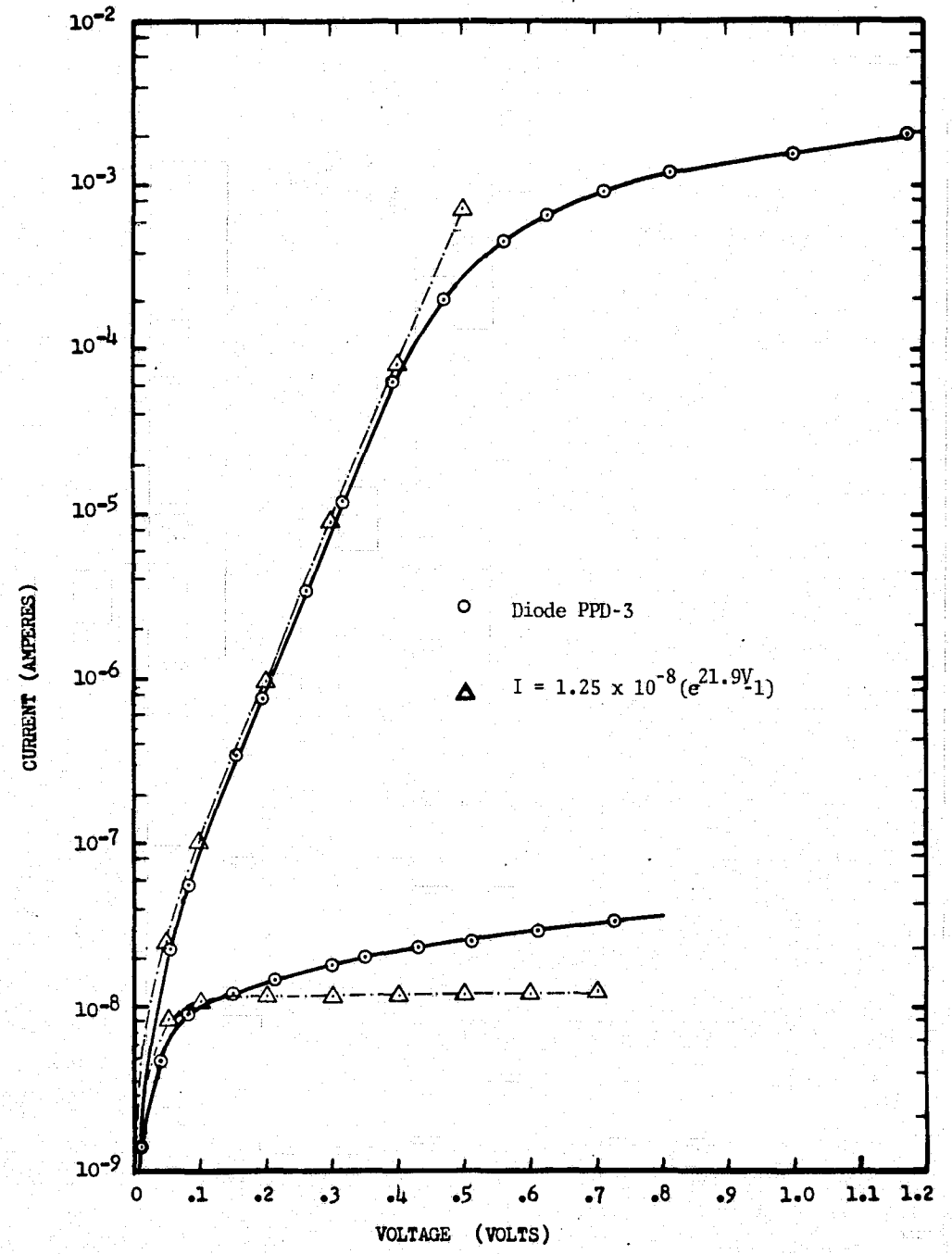


Figure 25. Current-Voltage Characteristics of Diode PPD-3 (the lower trace is the reverse characteristics)

that the reverse current and the forward current at low current densities are dominated by generation-recombination (g-r) currents. The theory does not give a simple formula of the above form.

Sah, Noyce and Shockley[2] derived expressions for the g-r currents and compared them with experiments on diffused silicon diodes. Their expression for the reverse current is the simplest:

$$J_{rg} = \frac{q\, n_i\, W}{2\sqrt{\tau_{po}\, \tau_{no}}\, \cosh \epsilon_t}$$

where

n_i = intrinsic carrier density

= 1.8×10^{-10} cm^{-3} in silicon at room temperature

W = space-charge width

τ_{po}, τ_{no} = excess carrier lifetimes in the space-charge regions

$$\epsilon_t = \frac{E_t - E_i}{kT} + \frac{1}{2} \ln \frac{\tau_{po}}{\tau_{no}}$$

where

E_t = trap energy

E_i = intrinsic Fermi level

In the above expression τ_{no} is the quantity of interest since it is the lifetime for minority carriers in p-type substrate and determines the minority carrier diffusion length. The values of τ_{po} and τ_{no} would have to be determined separately by fitting the theory at several points, including a point where diffusion current dominates. The latter is difficult in diode PPD-3 because of the appreciable series resistance.

The general expression for the current must be used for the forward current:

$$J_{rg} = \frac{qn_i W}{\sqrt{\tau_{po}\,\tau_{no}}} \quad \frac{2 \sinh q\,V/2kT}{q(V_o - V)/kT} \quad f(b)$$

where

$$b = e^{-qV/2kT} \cosh \varepsilon_t$$

V_D = the built-in voltage

The expression for f(b) in the general case of an asymmetric junction has been given by Choo.[3] If it is assumed that the value of τ_{po}/τ_{no} is near unity and that the value of cosh ε_t is less than 10, the value of f(b) for forward biases of 0.2 volt or more is close to the limiting value of $\pi/2$. Using this value gives an effective lifetime of

$$\sqrt{\tau_{po}\,\tau_{no}} = 9.1\ \mu\text{sec}$$

Needless to say, this value of effective lifetime may be quite incorrect. Examination of the reverse I-V characteristics in Fig. 25 shows that the reverse current is not proportional to junction width as expected from theory. Using the reverse current at 0.1 volt gives a value of cosh $\varepsilon_t = 17$ which is much higher than the values obtained by Sah, et al. We also note that they obtained very low values of effective lifetime in their n^+p devices (an average value of 52 sec). Thus the lifetime obtained in this way may not relate to the bulk lifetime.

Future efforts in this area will be directed at lifetime and diffusion length measurements and their relationship to the I-V and photovoltaic characteristics.

Photovoltaic Characteristics

Figure 26 shows the measured forward I-V characteristics of photodiode PPD-3 at an illumination level of 100 mW/cm^2. As noted on the figure, the current is a linear function of voltage at higher voltages, characterized by a series resistance (R_S) of 231 ohms. An expanded view of the positive current region is shown in Fig. 27. As previously mentioned this photodiode was prepared using its as-grown highly reflective surface; thus the above characteristics do not benefit from an antireflecting (AR) coating of any nature. The diode has an I_{SC} of 0.35 mA or J_{SC} = 11.7 mA/cm^2 and a V_{OC} of 0.38 volt. Because of the magnitude of R_S, the fill factor (FF) = 0.564, and the conversion efficiency = 2.5% as calculated on the figure.

Figure 28 shows the measured forward I-V characteristics of the companion single-crystal control photodiode SPD-2. Note that these forward characteristics (as with PPD-3) were also measured at an illumination level of 100 mW/cm^2. It has an R_S of 35 ohms. An expanded view of the positive current region and the efficiency calculation are shown in Fig. 29. Because of the fabrication geometry, this diode also has a large R_S, although it does benefit from a substantially thicker base layer and of course is larger in area. It has an I_S of 3.0 mA or J_{SC} = 20.9 mA/cm^2 and V_{OC} = 0.485 volt. Its FF = 0.503, and its conversion efficiency = 5.09%, about twice that of the dip-coated photodiode PPD-3.

H. J. Hovel, in his review book on solar cells (Ref. 1, p. 75) notes that the series and shunt resistances and the contact area loss are determined largely by fabrication technology rather than material properties. The reflection of the incident light can be minimized by proper antireflection (AR) coatings. He points out that it is useful to discuss the somewhat idealized conversion efficiency obtained by neglecting these technology-oriented losses, which he defines as "inherent efficiency." He reports (Ref. 1, p. 88) that if measured efficiencies are corrected for reflection, contact loss and series resistance

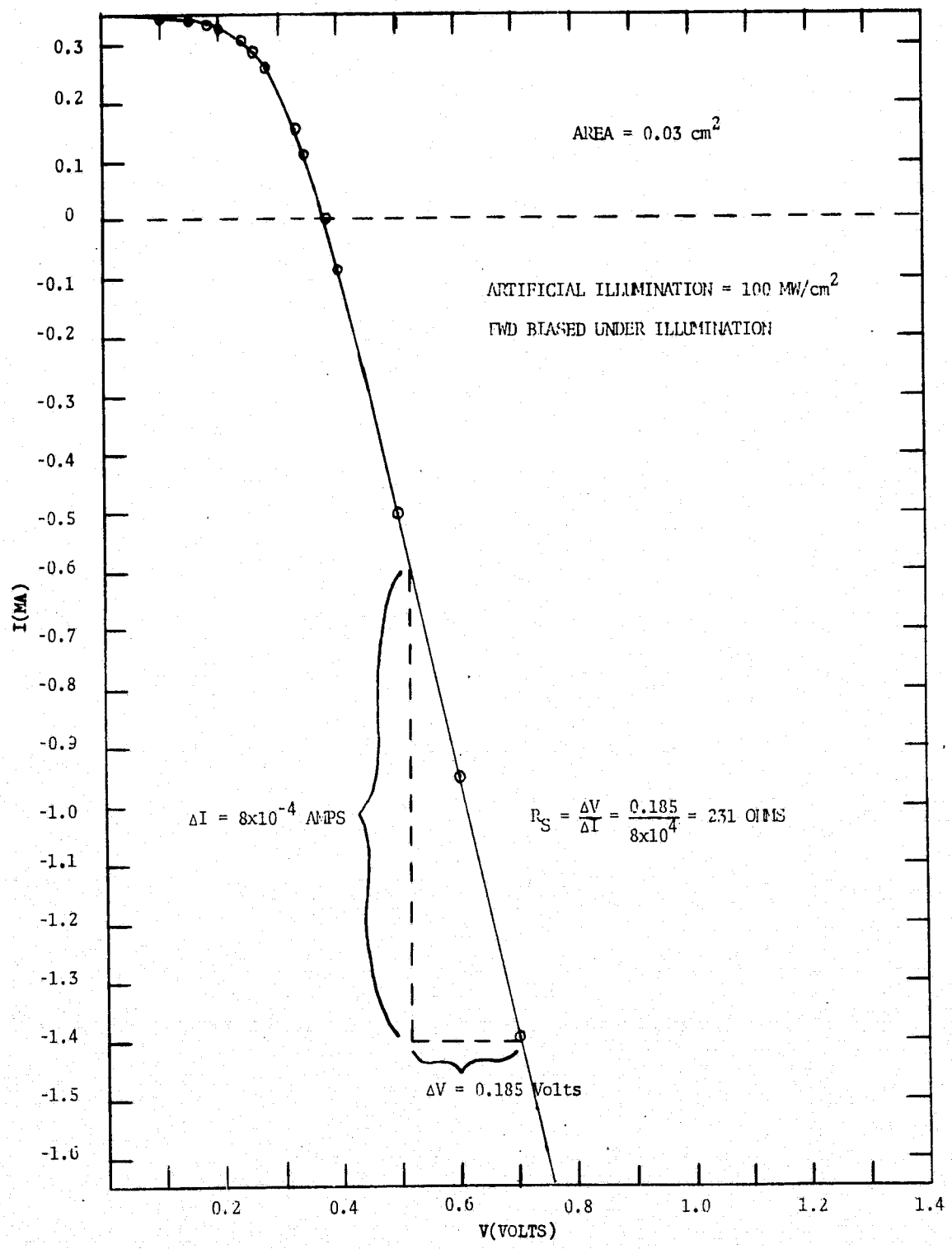


Figure 26. Illuminated Forward I-V Characteristics of Photodiode PPD-3

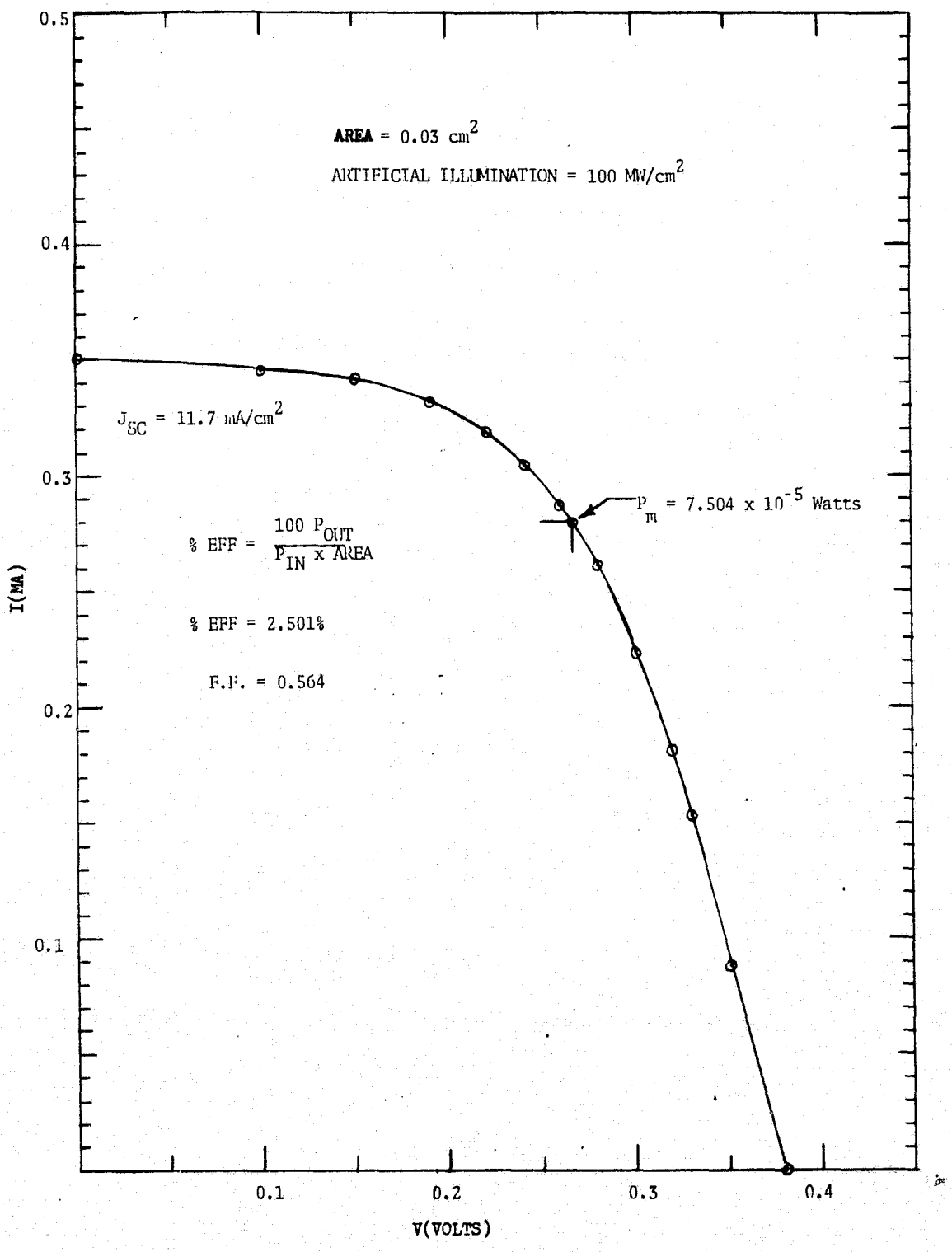


Figure 27. Photovoltaic I-V Characteristics of Photodiode PPD-3

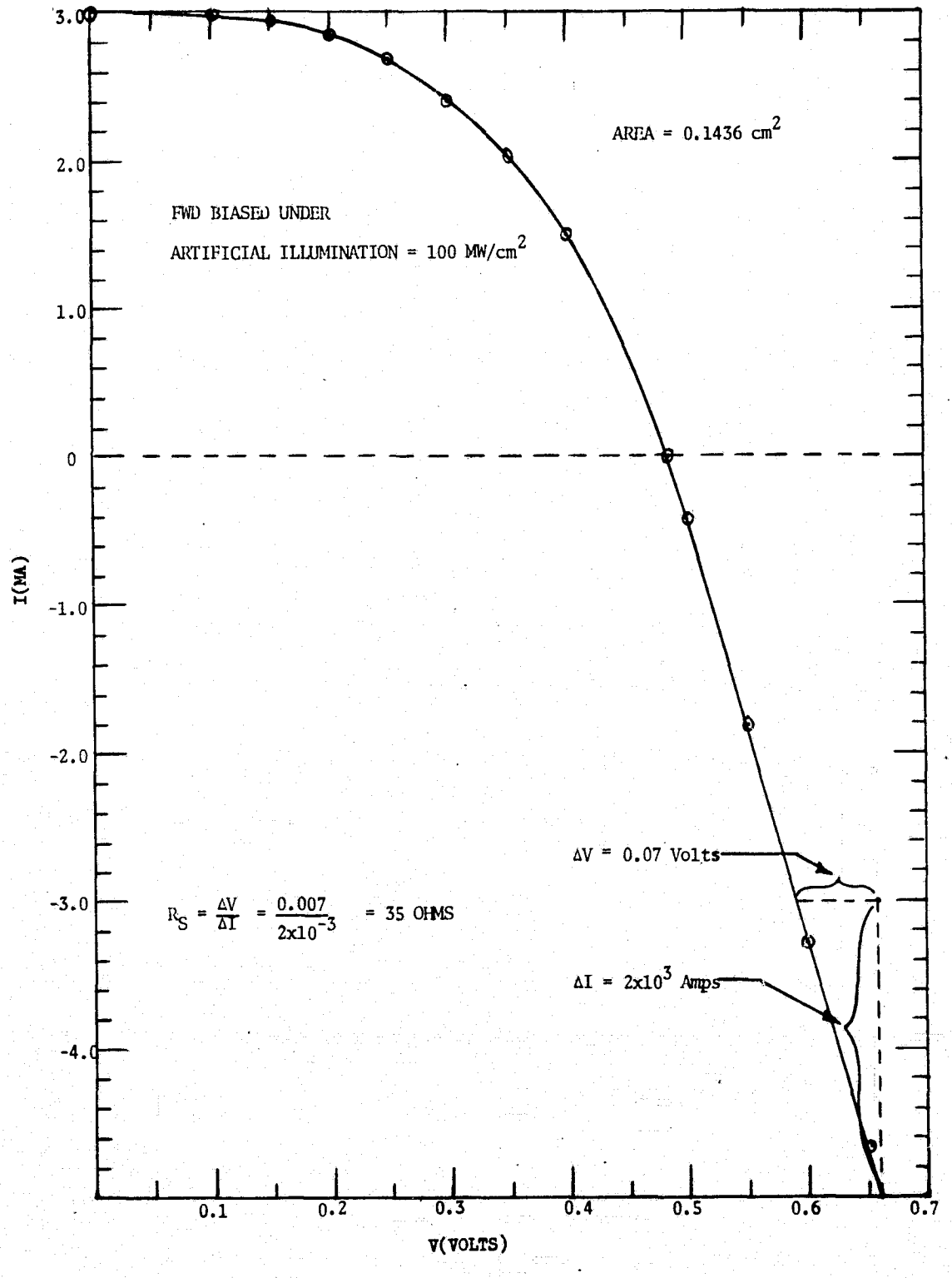


Figure 28. Illuminated Forward I-V Characteristics of Control Photodiode SPD-2

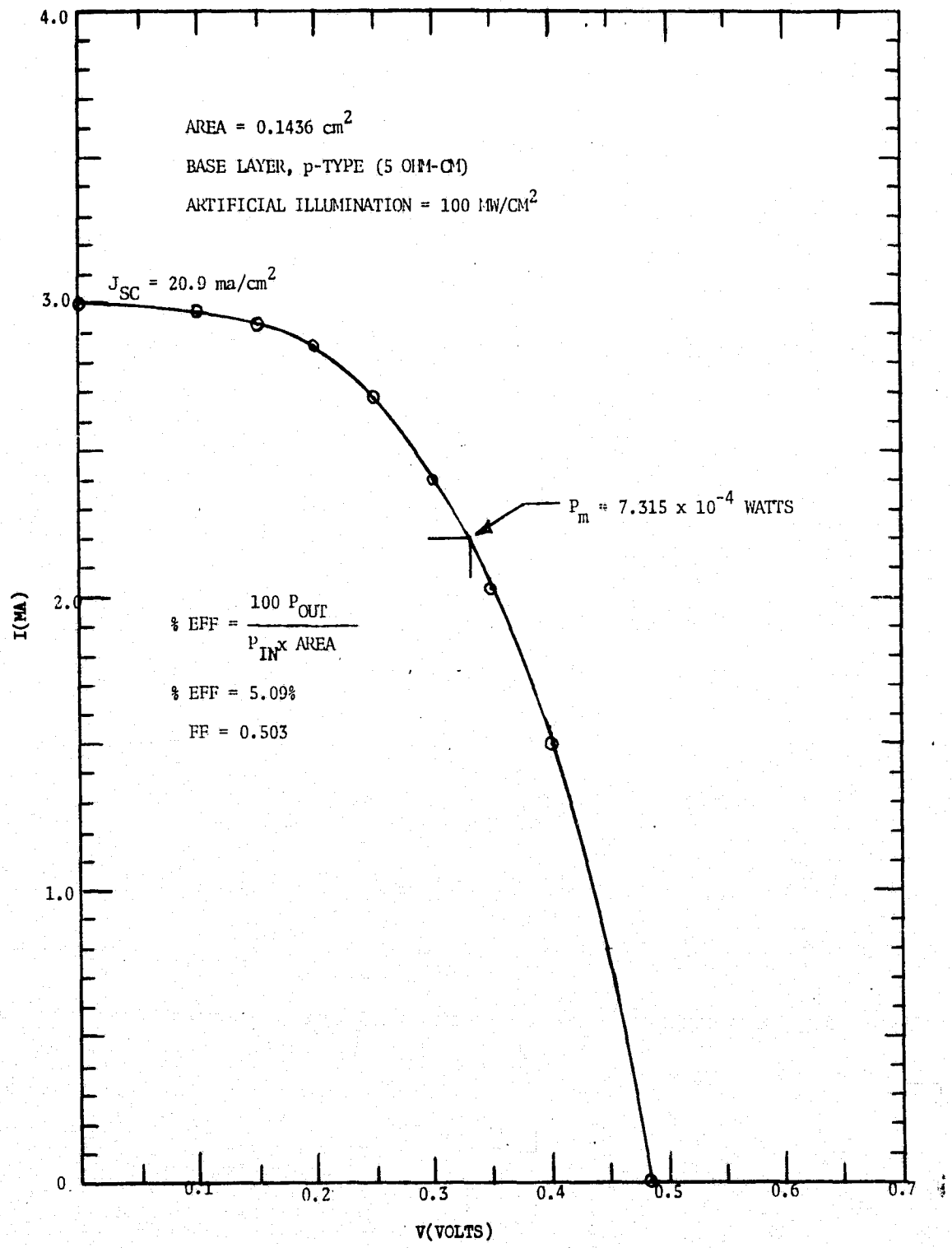


Figure 29. Photovoltaic I-V Characteristics of Control Photodiode SPD-2

loss, the results are in good agreement with calculated inherent efficiencies in silicon solar cells. He further notes (Ref. 1, p. 203) that in silicon, because of its large refractive index, the loss of incident light due to reflection amounts to 34% at long wavelengths (1.1μm) and rises to 54% at short wavelengths (0.4μm). Since the solar spectrum peaks near 0.55m to 0.6m, a reasonable estimate of the average reflective loss for the overall spectrum would be approximately 40% (Ref. 1, p. 203).

Using the above data, one can examine photodiode PPD-3, as well as the control photodiode SPD-2. Table 7 shows the correction for reflective loss and series resistance of both photodiodes.

Figure 30 is a plot of the adjusted photodiovoltaic I-V characteristics of PPD-3. After adjustment, J_{SC} is increased to 16.5 mA/cm^2, and the inherent efficiency was 4.84% with a FF of 0.774. The adjusted photovoltaic I-V characteristics for the control photodiode SPD-2 are shown in Fig. 31. Here J_{SC} = 29.4 mA/cm^2 and the inherent efficiency was approximately 10%.

Some optimization is yet to be performed on surface concentration and junction depth, and, when this is accomplished, it should be possible to expect conversion efficiencies in excess of 5% from present state-of-the-art dip-coated layers once the cell parameters are more fully optimized.

Table 7. Adjusted Photovoltaic I-V Characteristics

Dip-Coated Photodiode PPD-3, R_S = 231 ohms			
V_M(volts)	I_M(mA)	$I_A = 1.4I_M$(mA)	$V_A = I_A R_S + V_M$(Vo)
0	0.35	0.49	0.113
0.1	0.345	0.483	0.211
0.15	0.341	0.477	0.26
0.18	0.336	0.47	0.289
0.2	0.327	0.458	0.306
0.24	0.305	0.427	0.339
0.26	0.287	0.402	0.353
0.28	0.26	0.364	0.364
0.33	0.152	0.213	0.379
0.34	0.11	0.154	0.375
0.38	0	0	0.38
Control Photodiode SPD-2, R_S = 35 ohms			
0	3.0	4.2	0.147
0.1	2.97	4.16	0.245
0.15	2.93	4.1	0.293
0.2	2.86	4.0	0.34
0.25	2.68	3.75	0.381
0.3	2.4	3.36	0.417
0.35	2.02	2.82	0.45
0.4	1.5	2.1	0.473
0.485	0	0	0.485

NOTE: V_M = Measured voltage

I_M = Measured current

V_A = Adjusted voltage (adding IR drop)

I_A = Adjusted current (added for lack of AR coating)

R_S = Series resistance

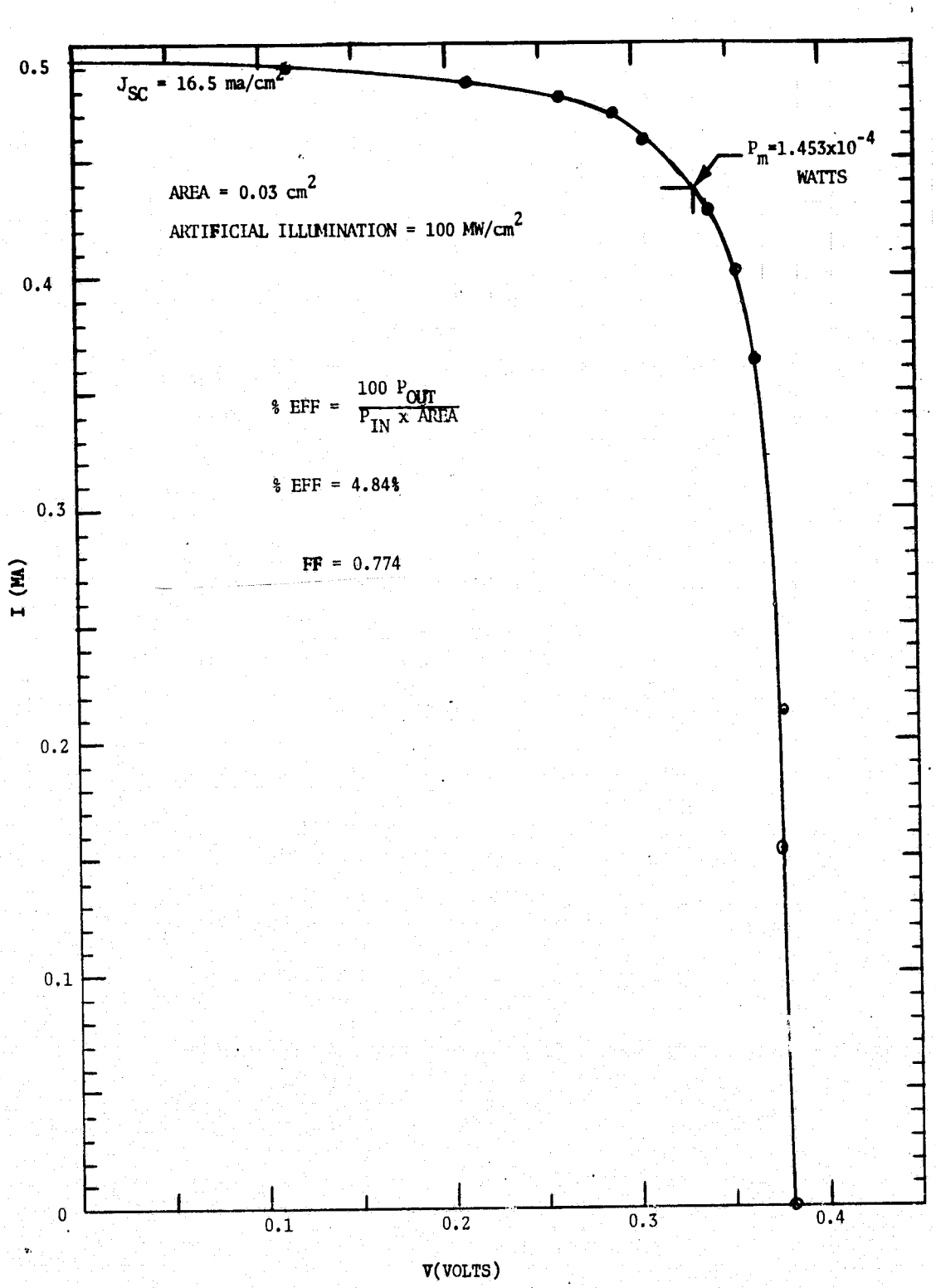


Figure 30. Adjusted Photovoltaic I-V Characteristics of Photodiode PPD-3

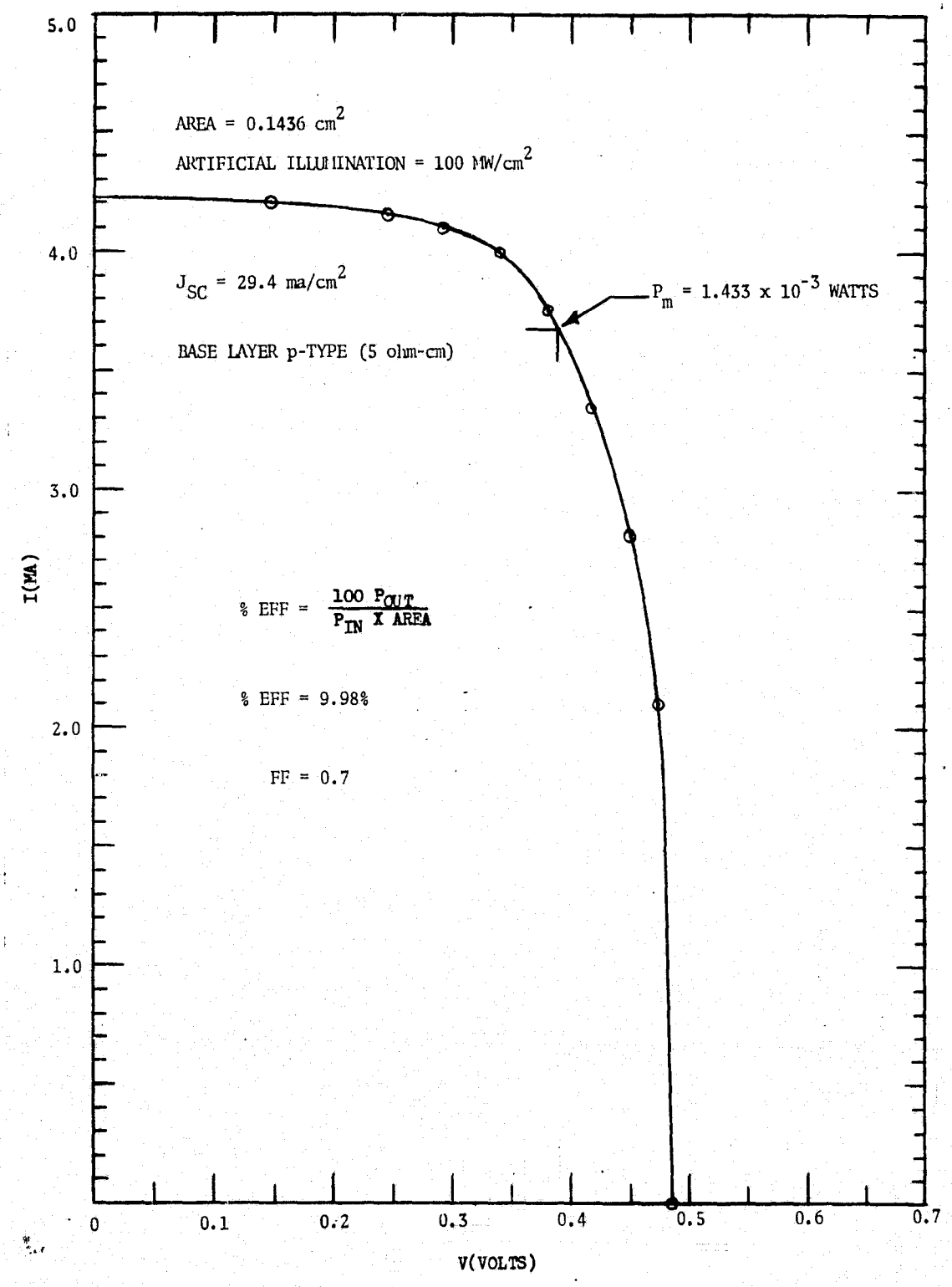


Figure 31. Adjusted Photovoltaic I-V Characteristics of Control Photodiode SPD-2

PROCESSING EFFORTS

The following processing efforts were carried out during the report period:

- A dip-coating facility was constructed for coating ceramic substrates with silicon. Substrates have been successfully processed with coated areas as large as $25cm^2$.

- A process was developed for growing thin sheet silicon having single-crystal grains with dimensions larger than the layer thickness.

- A low-cost process was developed for producing a ceramic substrate which is compatible with a dip-coating process.

- Processes were developed for applying the carbon film to the ceramic substrate. Not all of the processes gave films favorable for dip-coating.

- A process was developed for achieving excellent adherence of the silicon coating to the ceramic substrate.

- A process was developed for making electrical contact to the bottom of the silicon layer via the bottom side of the insulating substrate.

- A process was developed for diffusing a p-n junction into an as-grown silicon surface without prior costly processing steps.

- A process was developed (with varying success) for making electrical contact to this as-grown silicon surface following the function diffusion.

- A process is being considered to coat the ceramic substrate with a glassy carbon coating which is reported to be impervious to the diffusion of any impurities from the ceramic substrate.

- Processes are being considered for dip-coating at an angle (as opposed to vertical dipping) for the purpose of increasing the grain size and growth rate.

PROJECTION OF FUTURE ACTIVITIES

During the next six months our efforts will be directed at identifying and reducing the factors that limit the performance of solar cells coated on ceramic substrates. We will consider alternative coating techniques which minimize the exposure of the melt to the ceramic substrates so that low-purity, and hence low-cost, substrates may be used. The dipping technique has been very successful in getting large crystallites, and efforts to determine their dislocation density will continue. There will be an active effort to determine the extent to which the ceramic substrates contaminate the melt and the layers. Although we do not have in-house facilities, we will use different chemical analytical techniques to identify the types of impurities, their sources and the extent to which they affect solar cell performance. Higher purity mullite substrates will be evaluated to determine if higher performance can offset higher cost.

We will continue to seek to identify critical parameters in the graphite coating process. We expect to dip-coat glassy carbon coatings obtained from Tylan Corporation and to determine their degree of impermeability to impurities. Additional substrate carbonization techniques which produce thinner carbon films will be investigated.

The dip-coating facility has proved very versatile and will be upgraded with an improved temperature controller, and an after-heater will be installed to keep the coating process closer to the melting point of silicon. The dip angle will also be varied to determine optimum conditions for large grain size and increased growth rate.

The evaluation of dark I-V and photovoltaic properties of diffused junctions in dip-coated layers and control samples will continue. Independent

efforts to measure minority carrier lifetime, diffusion length and recombination centerproperties will be pursued.

The solar cell fabrication process will be upgraded by using improved diffusion parameters, electroding techniques and superior cell structures.

NEW TECHNOLOGY

During this reporting period there were two techniques developed which are believed to be technological firsts and could have an impact on the program's future:

- By dip-coating a mullite substrate having a narrow slit cut in it, it was demonstrated that silicon will seep through to the back side of the substrate. By preparing substrates with slits in them, as shown in Fig. 22, a new method is available for making contact to the base layer of solar cells.

- Dip-coated layers of silicon were placed on 5-mil-thick Graphoil, which is a product of Union Carbide and is a graphite foil available in several thicknesses. Pending determination of its economic feasibility, it may qualify as an alternative substrate material.

CHARACTERIZATION DATA SUMMARY

With the exception of American Lava's hot-pressed mullite, all the substrates dip-coated during this reporting period withstood the thermal shock of being immersed into molten silicon. Because of the marginally low melting point of cordierite, consideration was not given to dip coat it. Rolled, dried and fired mullite substrates, processed by Honeywell from McDanel's MV-20 plastic composition, do have a thermal expansion coefficient very similar to silicon. Excellent silicon coatings with good adhesion have been obtained on this substrate material. Unfortunately the electrical characterization data of these substrates indicate that it may slightly dissolve in molten silicon. Alumina substrates, while chemically purer, have either shattered upon cooling or have shown evidence of thermally stressing the silcon coating. The majority of the other ceramic substrates dip-coated have been eliminated as contenders in defining an appropriate substrate material. Polygranular SiO_2 and pressed "Fiberfrax" (mullite fibers) have not been adequately evaluated and thus could still be considered. It was experimentally demonstrated that molten silicon will "wick" through tiny slits in ceramic substrates making it possible to make electrical contact to the bottom surface of the silcon coating via the back side of the substrate. Sheet carbon and thin "Graphoil" also show technical promise as a substrate material candidate if they prove to be cost effective.

The adhesion of the silcon coating appears to be dependent on the thickness of the substrate carbon film as well as the substrate porosity. Bonding of the silicon to the ceramic is mechanical in nature, with the silicon penetrating the pores of the substrate and the carbon film apparently acting only as a wetting agent. Of the substrate carbonization processes tried, the carbon scrubbing technique, to date, has been the only method that has produced useful silicon coatings. Now that the nature of the silicon-ceramic interface is better understood, it is believed, however, that pyrolyzed carbonization techniques can also be made effective.

Silicon dip-coated layers have been grown with thicknesses ranging from a few microns to as thick as 0.011 inch. Their surface morphology and thickness are dependent on the pull rate and melt temperature. Presently useful layers 25μm to 75μm in thickness have been produced at pulling rates of 0.1 to 0.15 cm/sec in a melt 5° to 8°C above silicon's melting point. The layer's surface morphology is also dependent on the temperature above the surface of the melt. Without the use of a temperature-controlled after-heater, the nature of the films have indicated that supercooling of the melt existed in all cases before solidification. The films are dendritic in nature and on thicker coatings (50μm) have single grains typically 1mm wide tending to extend the length of the substrate with the long direction of the dendrites along the pulling direction. The crystallographic surface texture of the coatings are 1, 0, 0. The twin and grain boundaries usually run from the substrate to the surface of the coating indicating the coating consists mainly of a single layer of crystals. Crystallization of the coatings occur at the liquid-solid interface at an angle with the substrate that ensures continued nucleation from previously grown silicon.

The layers are p-type and have a resistivity range from approximately 0.7 to 2.0 ohm-cm when grown on McDanel MV-20 mullite substrates. They were intentionally doped to 5.65×10^{15} boron atoms/cm^3 (2.5 ohm-cm). The additional doping level has been shown to be aluminum acceptor atoms which are thought to originate from the mullite substrate. Hall mobility measurements made on samples fabricated so that current would run along grains in one and across grains in the other proved to be about one-half that of single-crystal material. The mobility of the sample with current crossing grains was slightly less.

Spreading resistance measurements have demonstrated that there is no detectable decrease in electrical conductivity across a twin boundary. Mesa-type photodiodes fabricated from various coatings have exhibited open circuit voltages as large as 0.38 volt and short-circuit current densities of 11.7 mA/cm^2.

These photodiodes, by virtue of their geometry, had an excessively large series resistance and had no antireflection coating. Allowing for this factor gives an inherent conversion efficiency of 4.84%.

The current voltage characteristics of the first photodiodes are dominated by excess recombination currents which lower the efficiency by decreasing the fill factor as well as the open-circuit voltage. At this time it is not clear whether the recombination centers are associated with impurities from the substrate or another source, or whether they are associated with grain boundaries. Identification and reduction of these centers is important in increasing the efficiency beyond the 5% level.

PROGRAM STATUS UPDATE

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Fig. 32, 33, and 34.

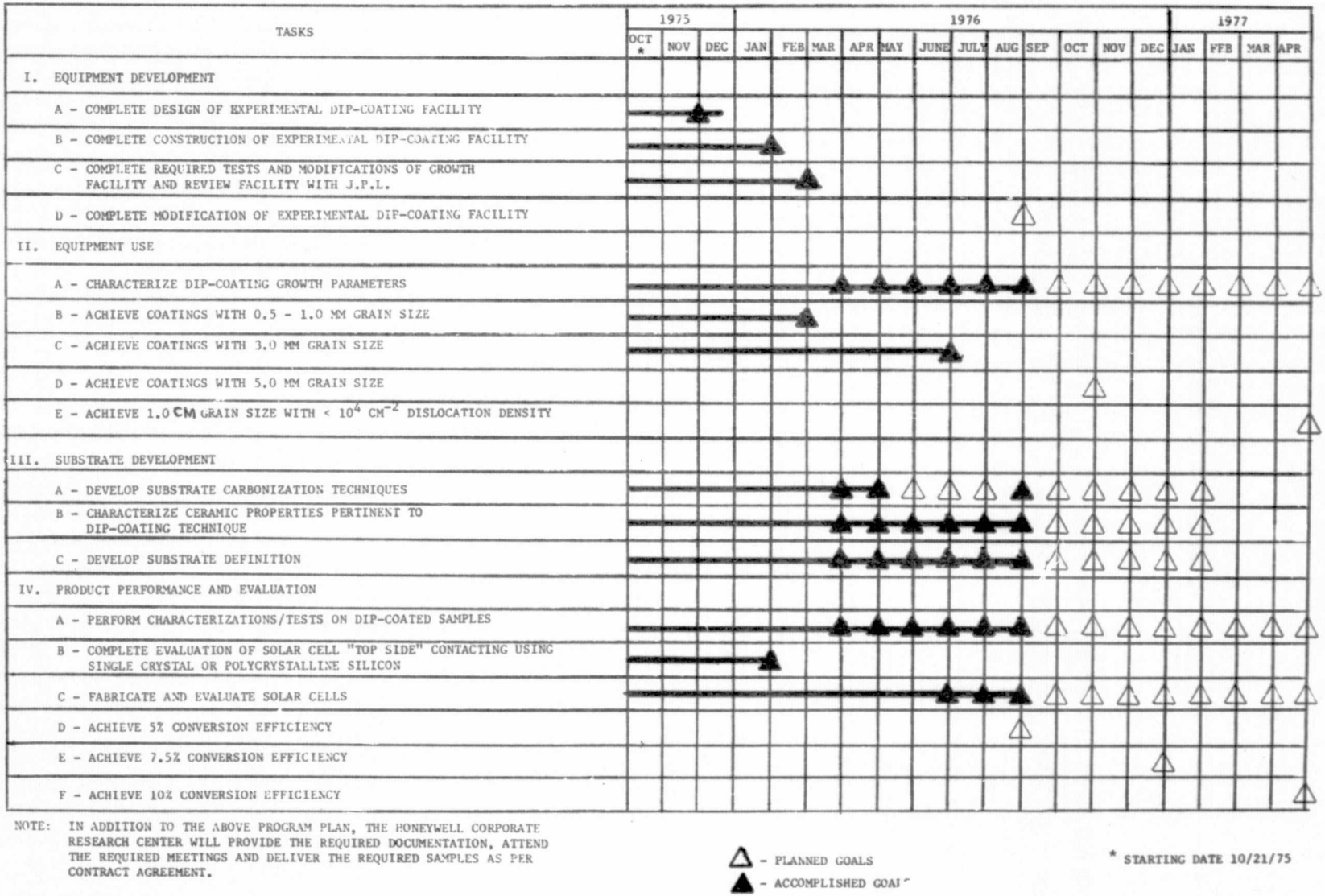


Figure 32. Updated Program Plan

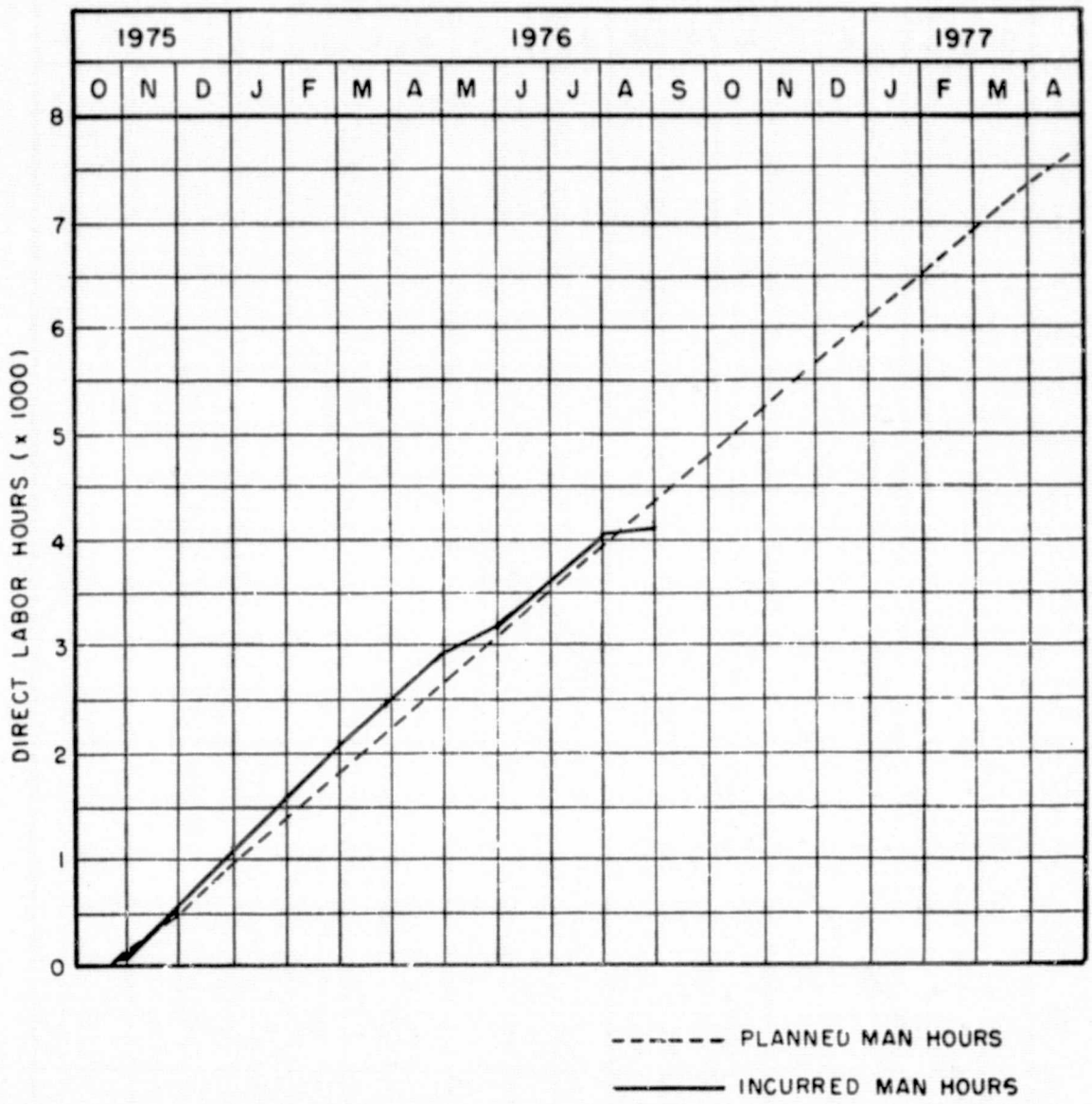


Figure 33. Updated Program Labor Summary

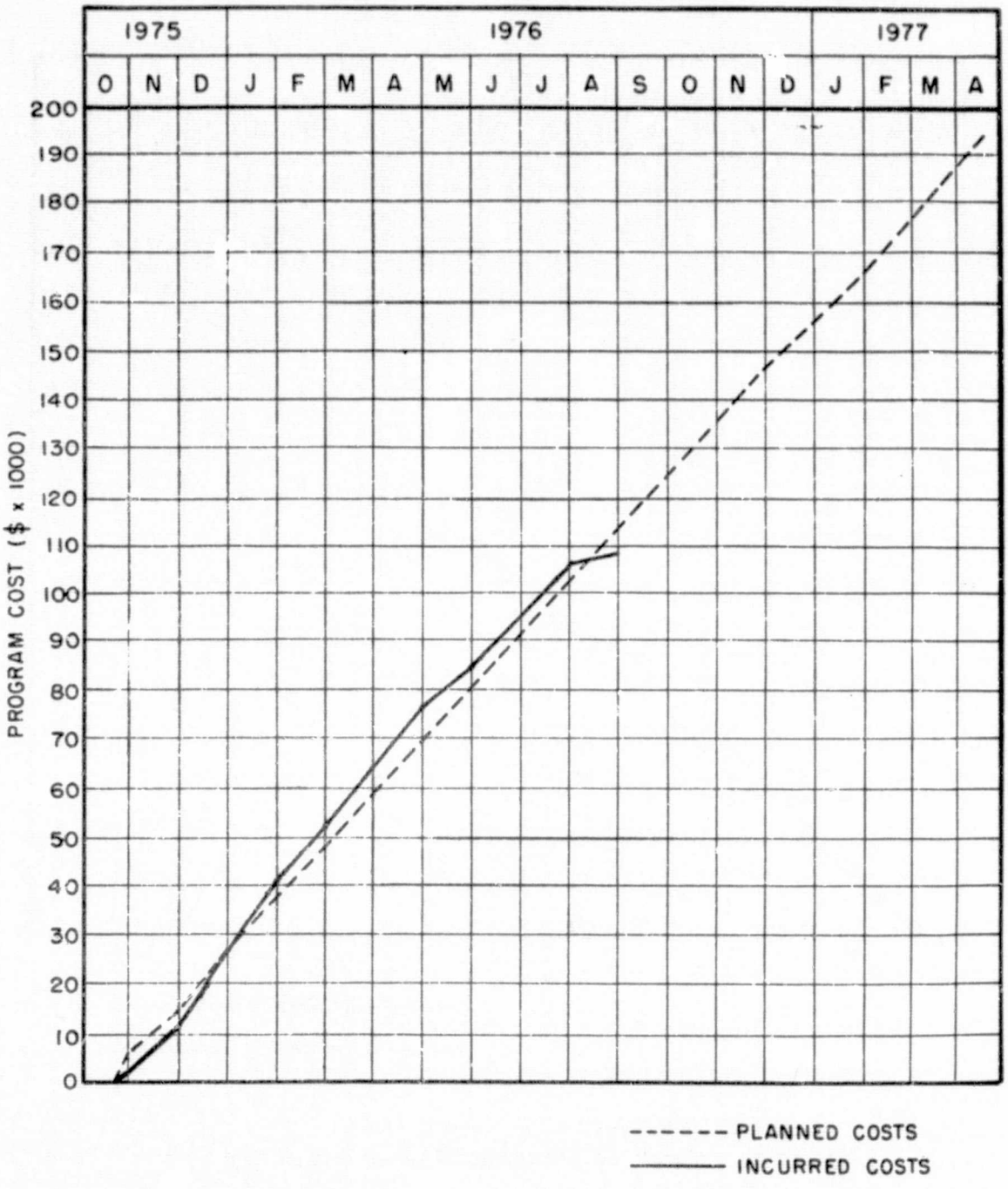


Figure 34. Updated Program Cost Summary

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